

LVL1 Trigger Status

on behalf of LVL1 Trigger Group*

Outline:

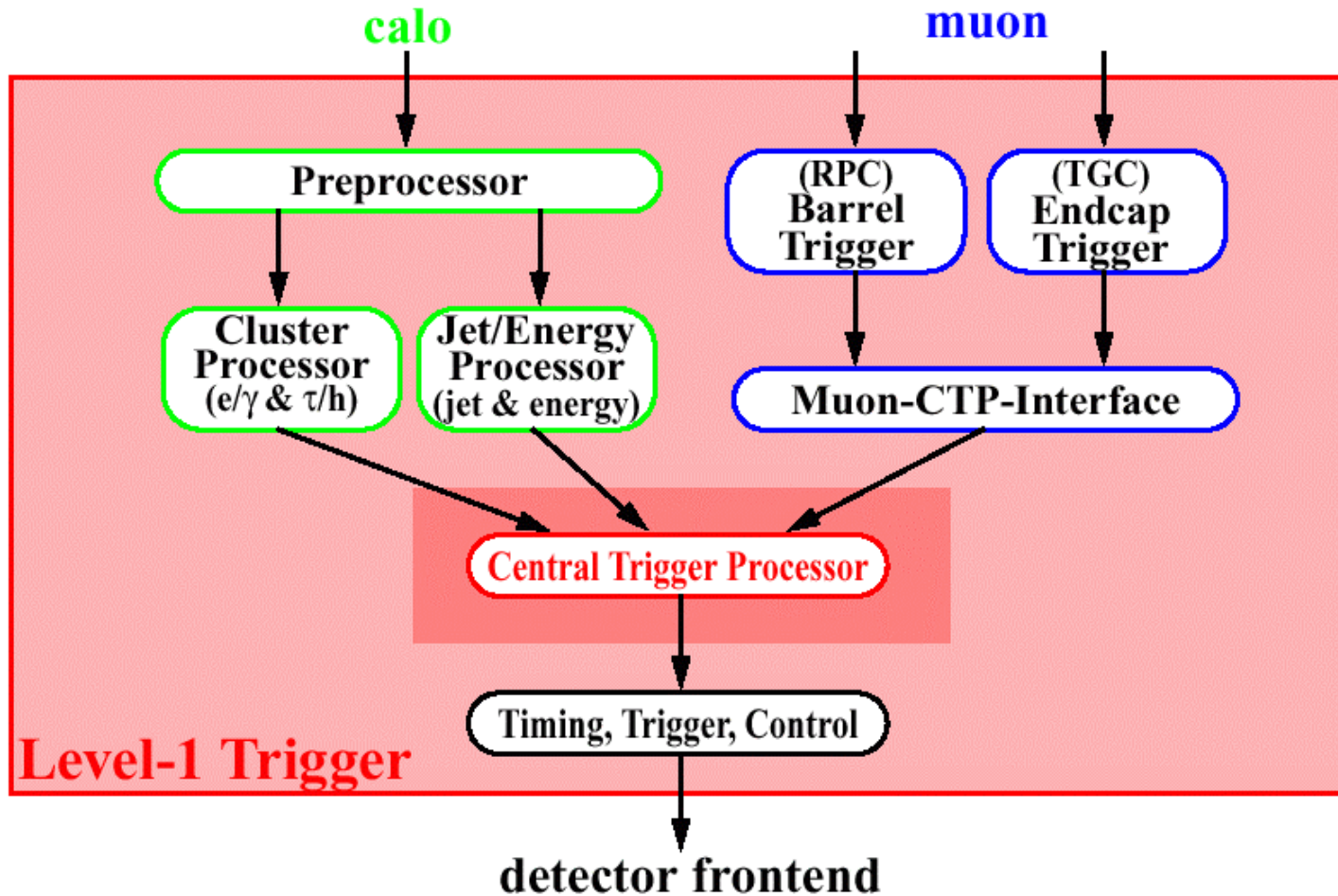
- ✧ Calorimeter
- ✧ Muon Barrel (RPC)
- ✧ Muon Endcap (TGC)
- ✧ MUCTPI
- ✧ Integration
- ✧ CTP

Chikara Fukunaga

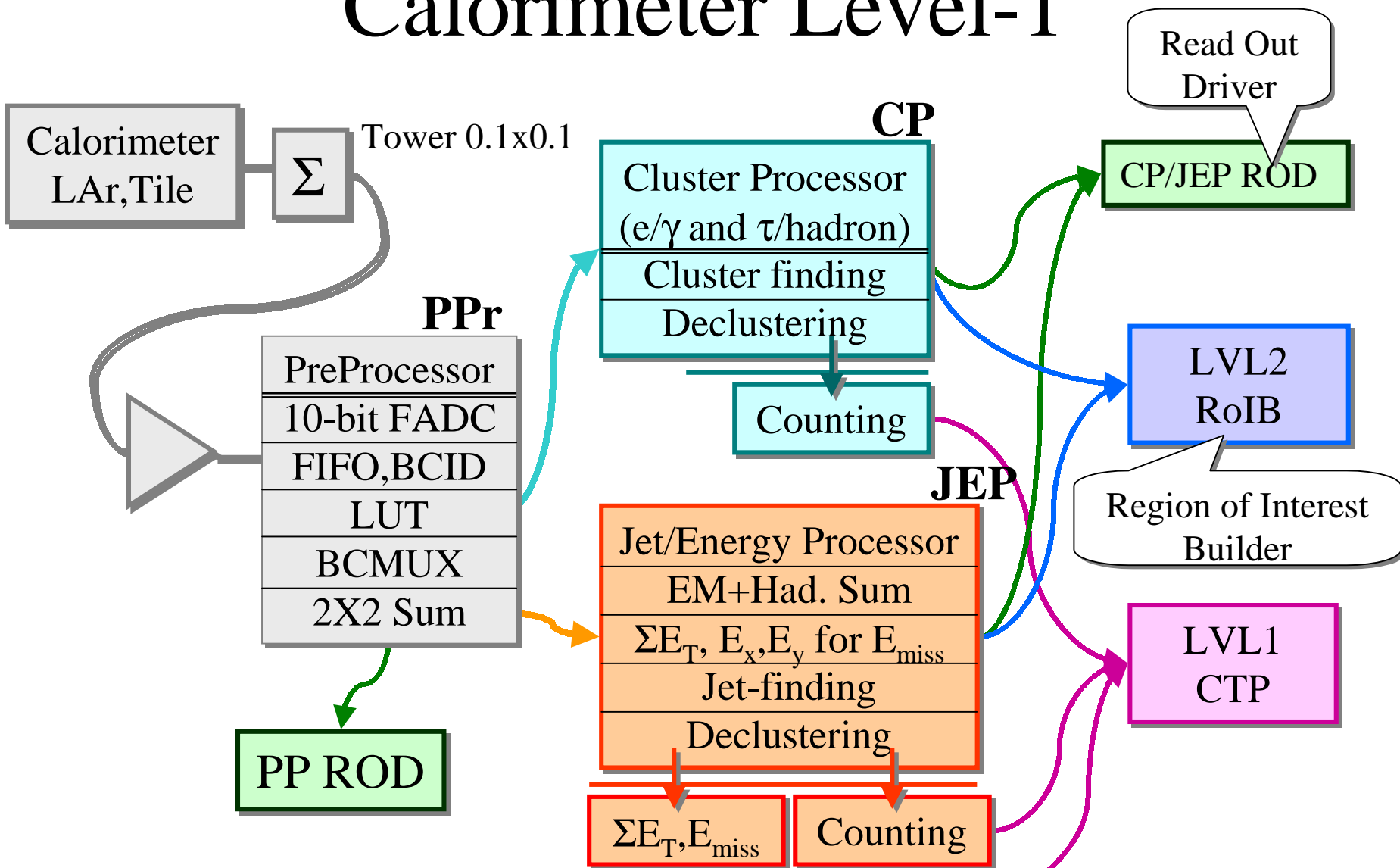
Tokyo Metropolitan University
(LVL1 End Cap Muon (TGC) Trigger group)

*in particular, with help from
E.Eisenhandler, N.Ellis, N.Gee, K. Hasuko, O.Sasaki, R.Spiwoks,
S.Veneziano, T.Wengler

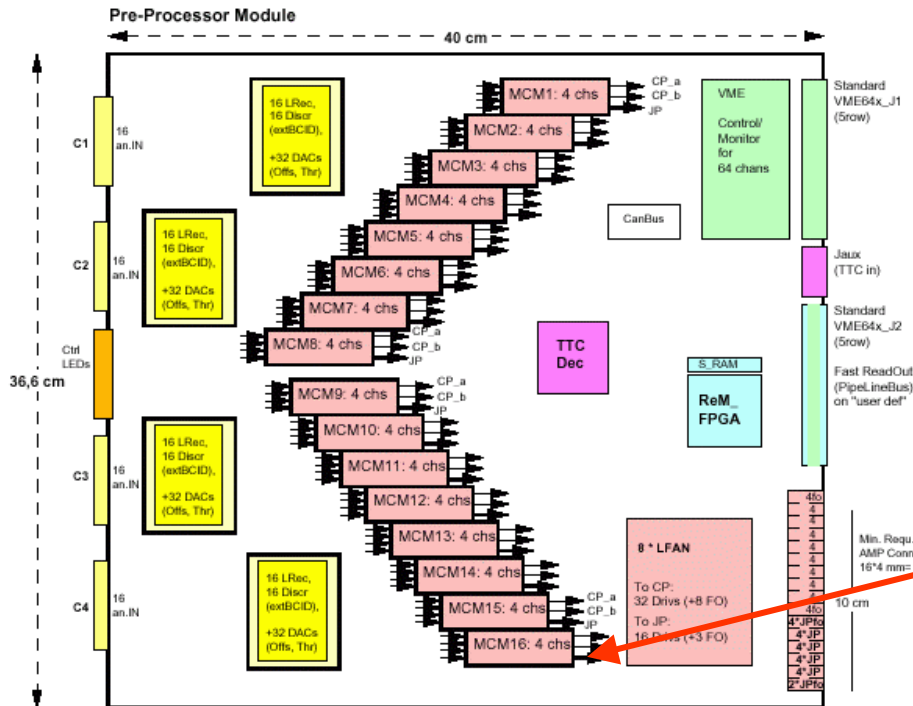
LVL1 Trigger



Calorimeter Level-1

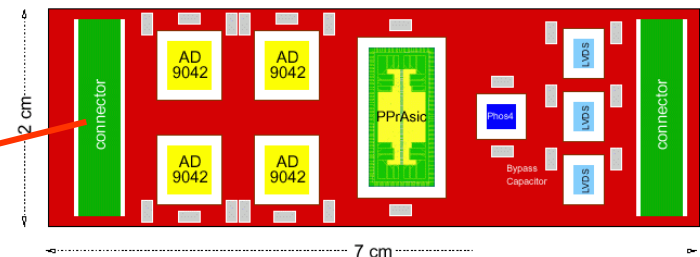


Preprocessor (PPr)



Pre Processor

- Calo. Tower ($\phi \times \eta = 0.1 \times 0.1$) Analog signal input, digitization, BCID, final E_T , thresh. cut, mask, $10 \rightarrow 8$ bit, BC Mux, 2×2 JET element, LVDS serialize



MCM :4FADC+PPrASIC

- **PPM**: Line Receiver, MCM, LVDS, ReM_FPGA (ReadOut I/F of PipeLine Bus to PPrROD) (PDR finished 3/'01 Full specification prototype Autumn/'01)
- **PPr ASIC** : BCID, LUT, BCMUX, 2×2 Jet elem. (FDR finished PRR 9/'01*)
- **MCM** (Multi-Chip Module) : 4 FADC + 1 PPrASIC (FDR finished PRR 11/'01*)
- **PPrROD**: (PDR finished 3/'01)

* After evaluation of Full spec. proto

Cluster Processor (CP)

Cluster Processor

- find e/γ , τ /hadron for $|\eta| < 2.5$
- Multiplicities for cluster/isolations: 8 e/γ , (8 τ /had. or 8 e/γ) thresholds
- Multiplicities to CTP, readout to DAQ, RoI to LVL2 via CP/JEP ROD

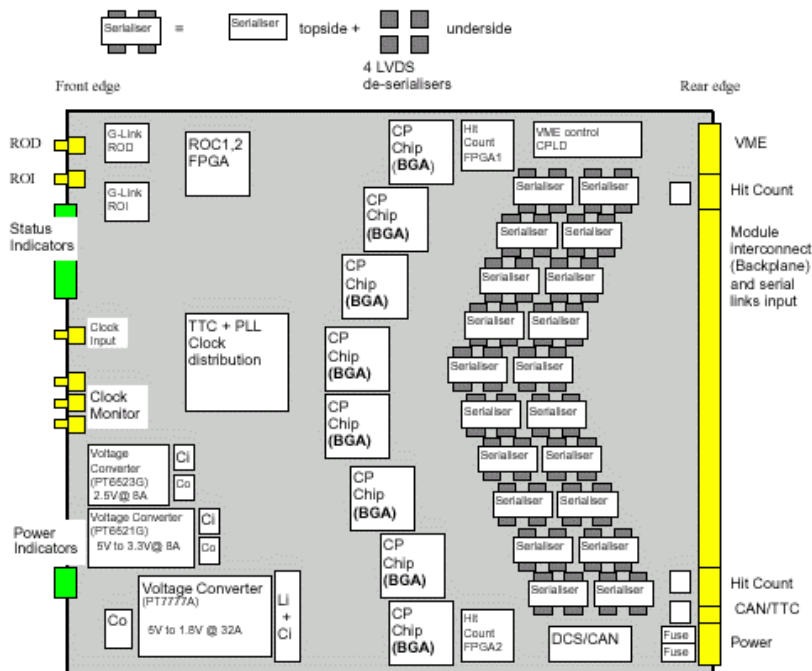
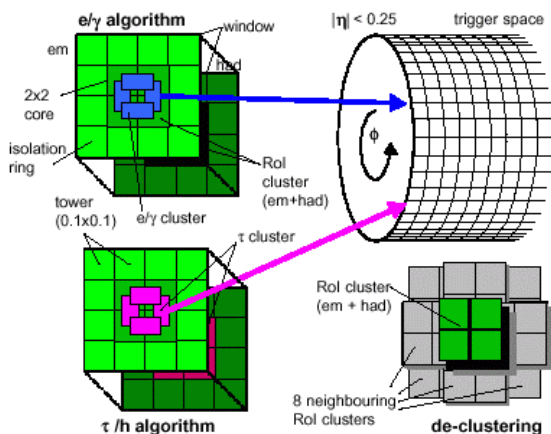


Figure 23: Approximate CPM layout and component footprint.

- **CPM:** 4x16 ($\phi \times \eta$) towers process, contains 20 Serializers, 8 CP chips
- Serialiser, CP chips are all now implemented in FPGAs
(PDR finished 7/'00, Full specification prototype will be built in Autumn/'01)

Jet/Energy Processor (JEP)

Jet Energy Trigger

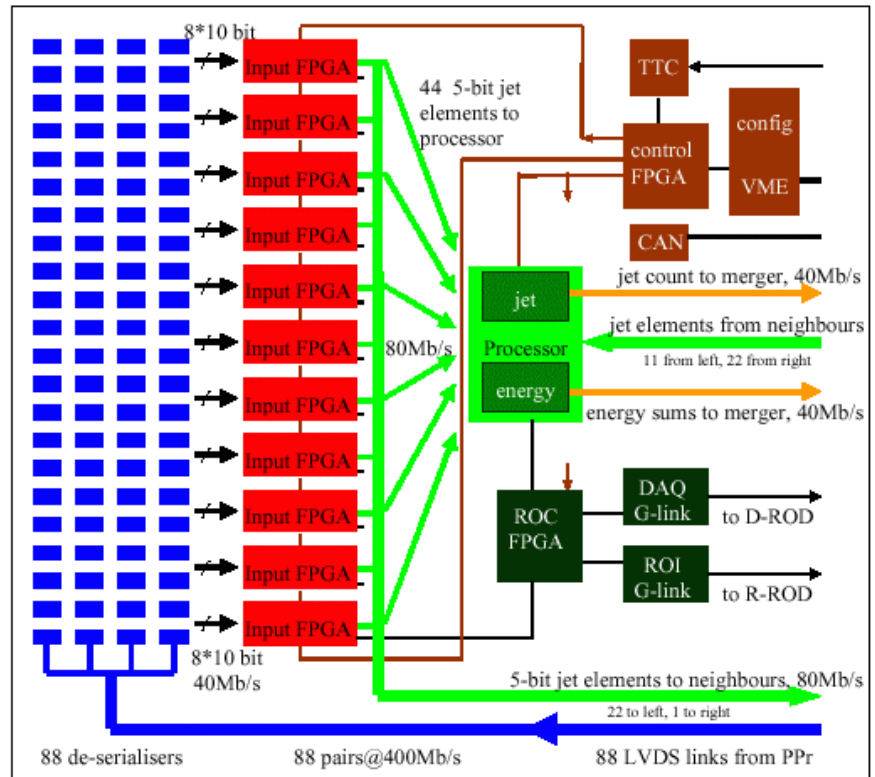
- Jet trigger $|\eta| < 3.2$ and FCAL jet trigger to $|\eta| < 4.9$
- Jet element 2×2 (0.2×0.2 ($\phi \times \eta$))
- Find jets programmable choice of 2×2 , 3×3 , or 4×4 windows, 8 thresholds.
- RoI based on 2×2 core
- Missing E_T , ΣE_T , to $|\eta| < 4.9$ incl. FCAL

Jet Energy Processor Module

- Covers 4×8 Jet element
- 11 Inputs, Jet processors are now FPGAs

(PDR finished in 12/'00)

(Full specification prototype will be built in Autumn/'01)



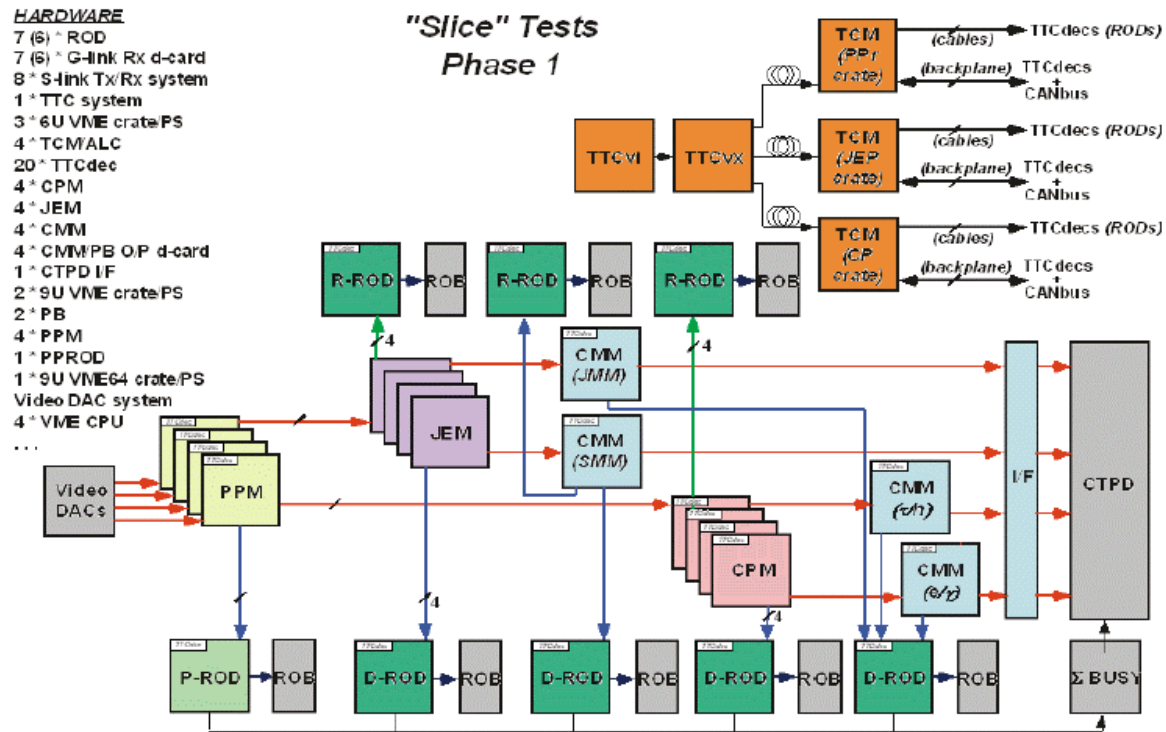
Jet Energy Processor Module (JEM)

Common Modules

- **Common Merger Module for CP, JEP** (PDR finished in 12/'00)
 - Counts e/γ and τ /hadron clusters for CP
 - Counts Jets for JEP
 - Calculates Missing E_T and ΣE_T
 - CTP I/F and RoI,DAQ ROD I/F

Full specification prototype will be built by Autumn/01
- **Timing Control Module for PP,CP and JEP** (PDR finished in 6/'99)
 - TTCsignal O/E and Fan-out for the Processors TTCrx
- **CP/JEP ROD** (Prototype PDR done, Full spec. PDR in 09/'02)
 - Receives RoI/Data from CP/JEP via G-link
 - RoI/DAQ Readout Data to ROB via S-link
 - 6U 4-channels proto. module available (Final 9U 16-channel)
 - Integration Test with ROS and RoIB was done in 04/01

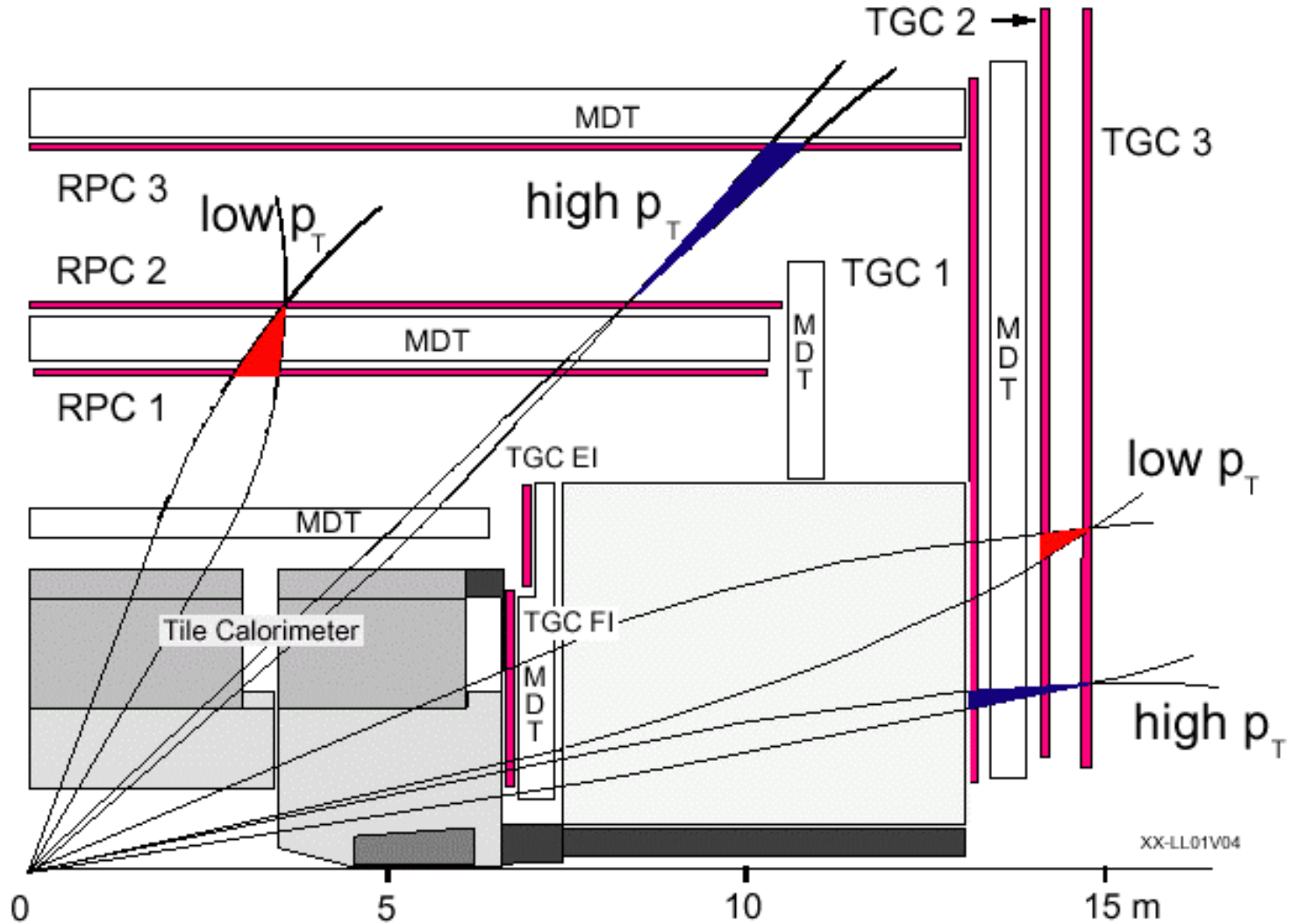
Slice test Phase1 starting Autumn 2001



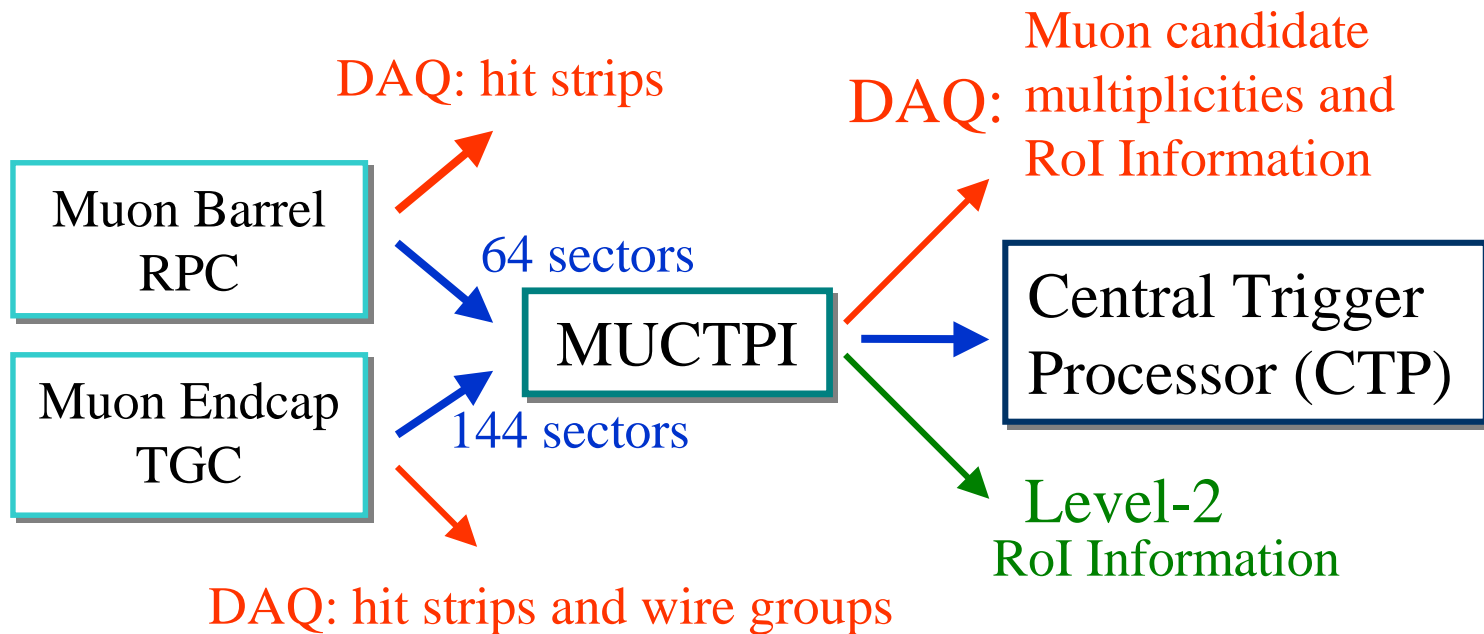
- Phase 1 Slice test

- 1/14 of the barrel
- With prototype CP/JEP ROD
- Data Acquisition soft based on tools from ATLAS Online Software project
- With Linux based VME single-board PCs.

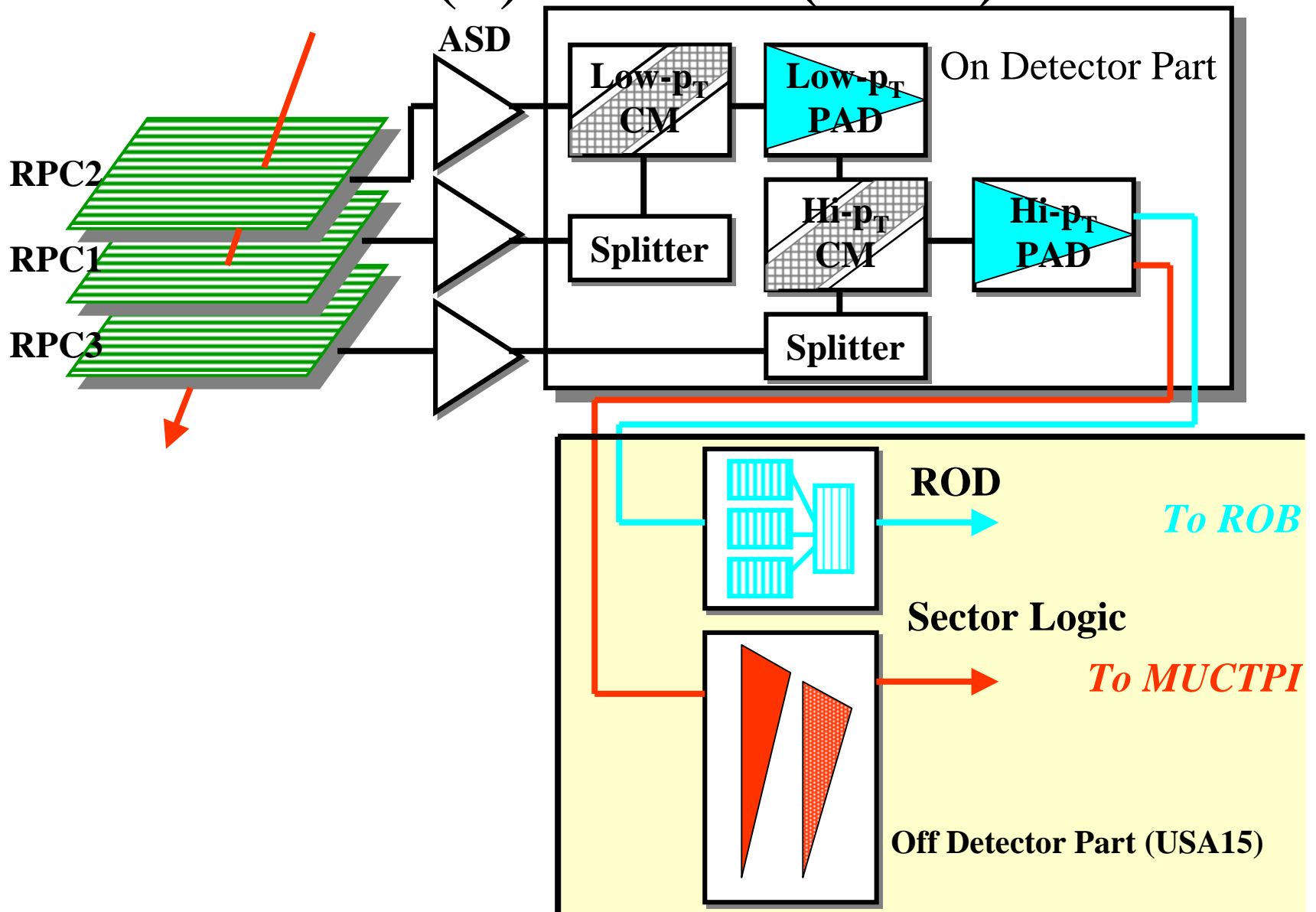
Muon Level1 Strategy



Muon Trigger Level-1 System Structure



Muon(1): Barrel (RPC)



Current Status (I)

◆ Coincidence Matrix (CM) ASIC (CMA)

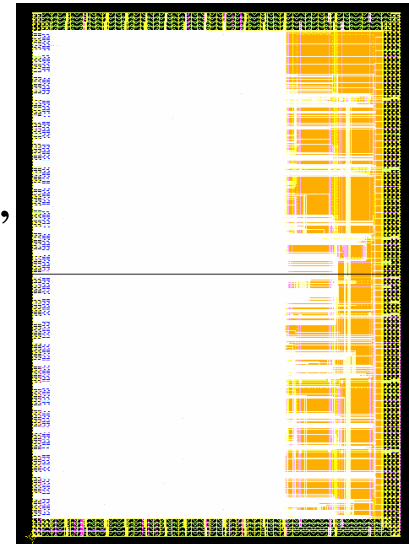
PDR done (Jul.'00)

- Coincidence of RPC1 & RPC2 for low- p_T , and low- p_T & RPC3 for Hi- p_T
- UMC (United Microsystems Co;) 0.18 μ m standard cell
- Preliminary floor plan and P&R (Place and Routing) finished
- Aim of submission on MPW 15 September 2001

◆ PAD prototype

PDR done (Jul.'00)

- Combination of η and ϕ , solve overlap in PAD (0.2x0.2), select highest p_T candidate, and readout buffer, derandomizer+optical Tx
- Prototype-0 under assembly (wait for CMA)
- Main logic will be implemented in Virtex FPGA
- Tests forseen in Q3-4,2001
 - Device Initialization via DCS, JTAG, TTC timing,FE connection



CMA mask

Current Status (II)

Sector Logic Demonstrator CES MFCC

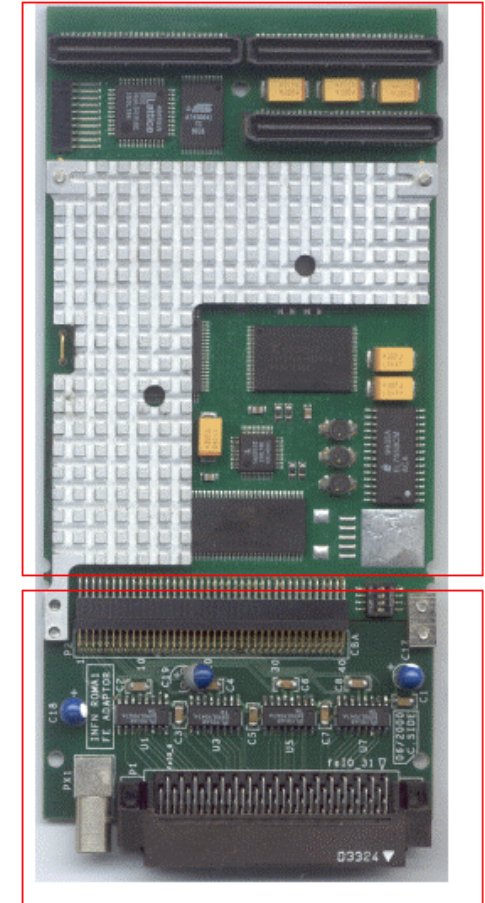
◆ Splitter Board

PDR done (Jul.'00)

- Electrical fan-out between ASD and CM
- Design of 40-channel prototype finished, PCB in production
- Design of Splitter power distribution board started

◆ Sector Logic Demonstrator

- 5-stage Pipe-line processor of (1) Low p_T filter, (2) TileCal coincidence, (3) sector overlap solving, (4) and (5) two highest p_T candidates
- Demonstrator board based on CES RIO2 + MFCC (PMC with PowerPC and Altera FPGA) + LVDS adaptor (32 bit) nose
- Integration test with MUCTPI will be in the summer 2001
- PDR in Jul.,2001



MUCTPI I/F

Current Status (III)

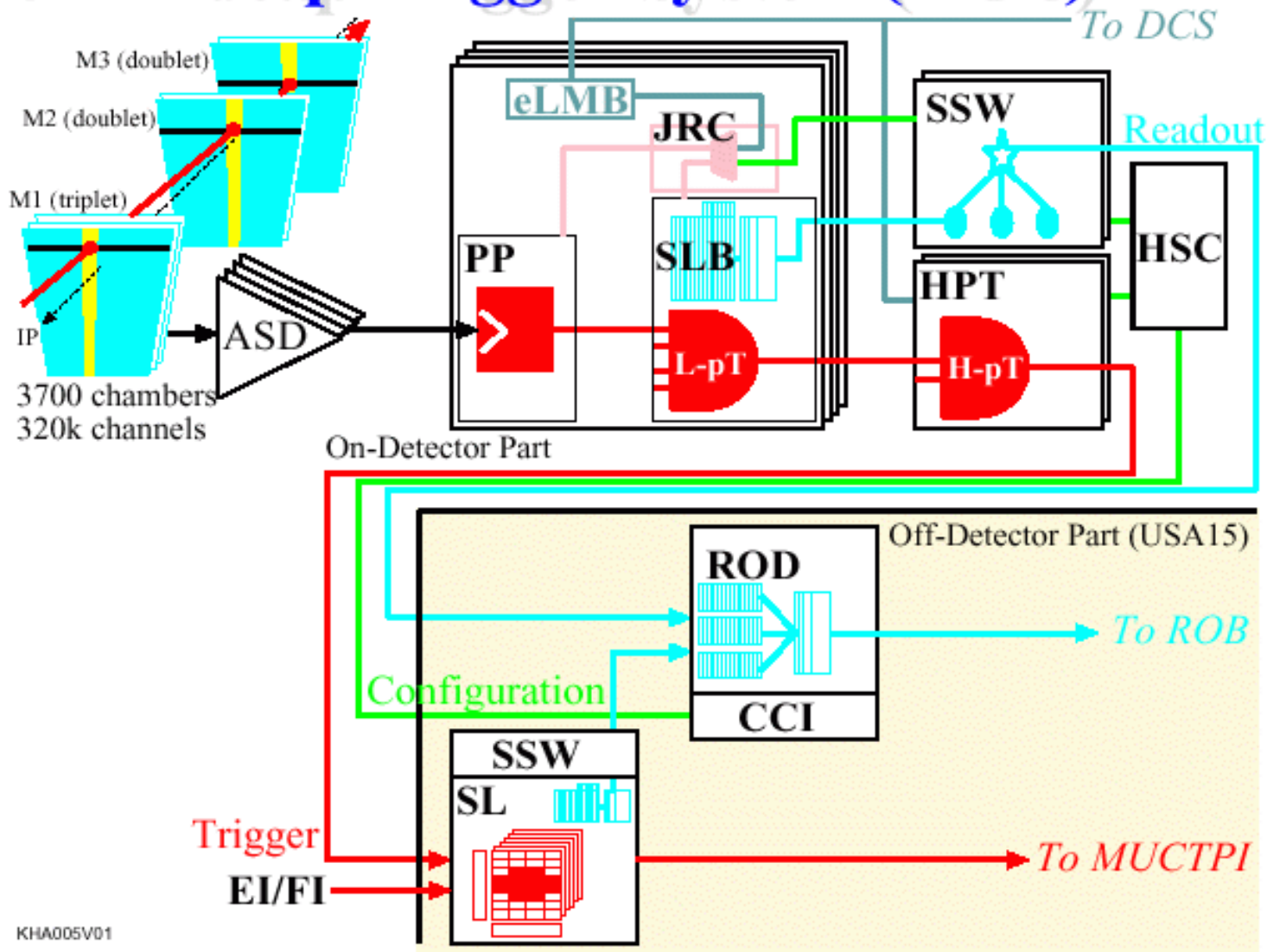
◆ ROD

- Design for 6U VME system of Link Rx board (for SL,ROD) started
- PDR in July 2001

◆ Slice Test

- ASD → splitter → CM(low p_T) → CM(Hi p_T) → PAD(tx) → rx → SL&ROD + DCS, TTC
 - using prototype
 - Partial Integration will begin late 2001
 - Full slice test will be started in Q1-2, 2002

Muon Endcap Trigger System (TGC)



Current Status (I)

◆ ASIC Prototyping in VDEC

- VDEC: VLSI Design and Education Center (University of Tokyo)
- Open to Japanese universities for academic use
- Share a mask pattern with different designs ⇒ can save fabrication costs
- Fabrication cycle: 1~3 times/year

◆ Patch Panel (PP)

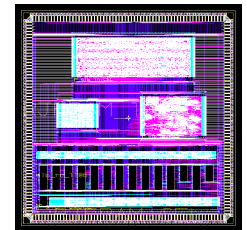
PDR Done (Jun'00)

- PPIC: BCID, fine delays, Test-Pulse Generator for ASDs, LVDSrx
- PPIC-ver.3: ROHM 0.6 μ m CMOS full-custom (4.5mm \times 4.5mm)
full-specification; DLL → PLL; small bugs fixed
submission in Jun'01; delivery in Oct'01

◆ SLave Board (SLB)

PDR Done (Jun'00)

- SLBIC: local coincidence logic (3/4, 2/3 and 1/2)
LVL1 readout buffer and derandomizer for intermediate hits
- SLBIC-ver.0: ROHM 0.35 μ m CMOS full-custom (9.7mm \times 9.7mm)
full-specification version, 350k gates
delivered in May'01; now in test

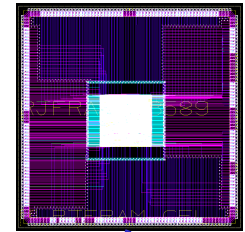


Current Status (II)

◆ High-pT Board (HPT)

PDR Done (Jun'00)

- HPTIC: high-pT coincidence logic (r , ϕ)
- **HPTIC-ver.1'**: HITACHI 0.35 μ m CMOS gate array (4mm \times 4mm)
full-specification except for output format
delivered in Mar'01; tests almost done
- **HPTIC-ver.1**: ROHM 0.35 μ m CMOS full-custom (9.7mm \times 9.7mm)
full-specification version
delivered in May'01; now in test



◆ Sector Logic (SL)

PDR Done (Jun'00)

- R- ϕ coincidence, track selector, readout block (using SLBIC)
- **SL-ver.0**: built using Virtex FPGAs as 9U VME64x
full-specification version for a forward sector
submission in Jun'01

◆ Other ASICS

- JTAG Route Ctler (JRC)-ver.0
- TTC Emulator-ver.0
 \Rightarrow ROHM 0.35 μ m; submitted in Feb'01; delivery in Jun'01

Current Status (III)

◆ Star SWitch (SSW)

PDR Done (Feb'01)

- Relay module for readout and configuration
LVDS (\leftrightarrow SLB), S-link (\rightarrow ROD)
- **SSW-ver.1**: built using Virtex FPGAs as special 9U VME
full-specification version
design finished; submission in Jul'01

◆ ROD

PDR Done (Feb'01)

- **ROD-ver.0**: almost full functionalities built using XCV405 as 6U VME
board being debugged; first-level FPGA design
- **Test ROD**: for SSW tests; 13 FE link ports, TTCrx, 1 S-link to ROB,
HITACHI RISC SH-4 (167Hz) as 9U VME64x
being debugged; available in Jun'01

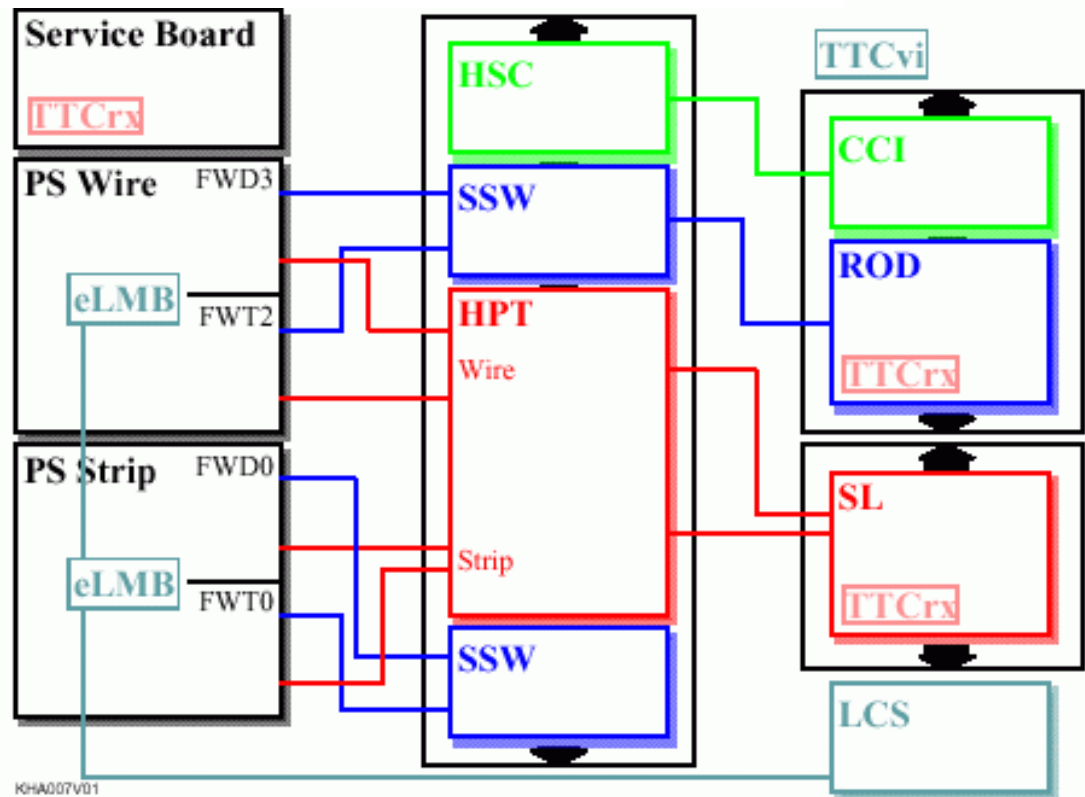
◆ HSC/CCI/DCS

PDR Done (Feb'01)

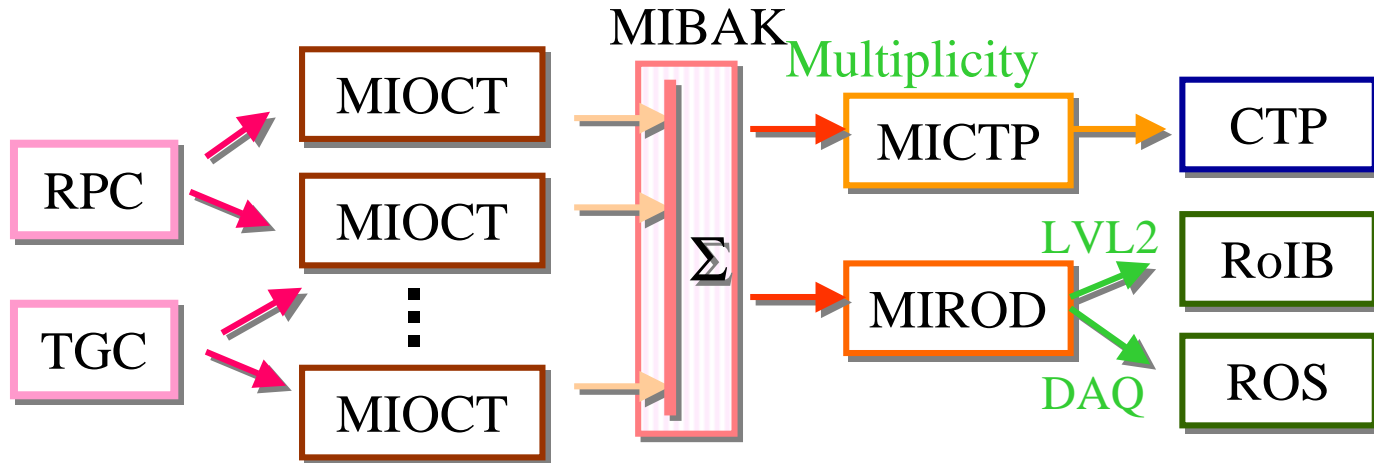
- **HSC/CCI**: VME controller for HPT/SSW crates to configure and restore
FPGAs in SSW (countermeasure for SEUs)
ver.0: built using CPLDs; debugs almost done; available in Jun'01
- **DCS**: **DCS board-ver.-1**; eLMB, Chamber Charge Monitoring Circuit
CCMC works well
PVSS-OPC-CAN(open)-eLMB-JTAG established

First Slice Test

- Start from September 2001
- 1/4 of a forward sector



Muon(3): Muon CTP Interface - MUCTPI



- **MIOCT** – Octant Board
 - Receive candidates from Sector Logic modules, solve overlap of Barrel and Endcap sectors (Overlap programmable)
- **MIBAK** – Backplane
 - Special active backplane dedicated for multiplicity summation, data collection, Timing signal distribution
- **MICTP** – CTP Interface
- **MIROD** – Readout Driver – Interface to RoIB and DAQ

MUCTPI Demonstrator

PDR for final MUCTPI done in 02/2001 at CERN


Module	Number	Comments
MIOCT	2	Full function for 14 Sectors but fixed (not programmable) overlap regions + emulator cards for MIBAK (test data generation)
MIBAK	1	Full function of dedicated back plane
MIROD	1	Full function +Test pattern RAM(2Hz-1MHz) for event Xmission
MICTP	1	Under-design , currently emulator card for multiplicities and busy signal extraction from MIBAK

Integration with RPC/ TGC from Q3,2001

Final design by July 2001

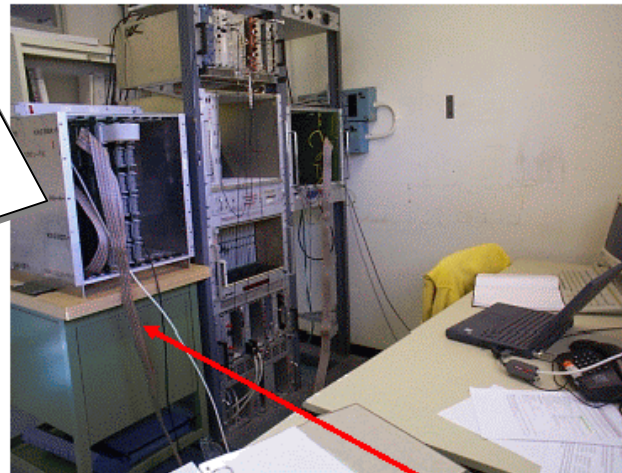
Integration test of MUCTPI (1)

Done in 2/'01

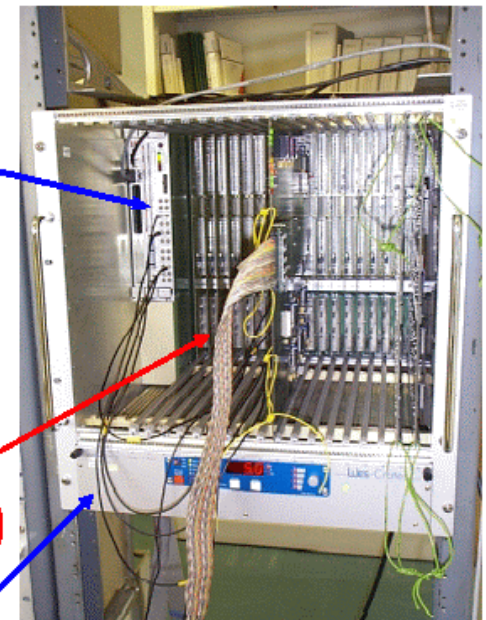
- MUCTPI-RoIB
 - MIOCT,MIROD **Data**  **BUSY** RoIB
 - MIROD – RoIB was up to 40KHz (100KHz) with(out) data verification
 - L1A at MIOCT to RoIB in was $\sim 2.6\mu\text{s}$
 - BUSY signals from RoIB could control MIROD data flow

12U VME crate

- S-link input card
- 2 processor cards for RoI building
- 2 RIO2s for LVL2 Supervisor & Crate Processor



The RoIB crate (left) and the MUCTPI crate (right)



Front view of the MUCTPI crate

Slink cable MUCTPI – RoIB

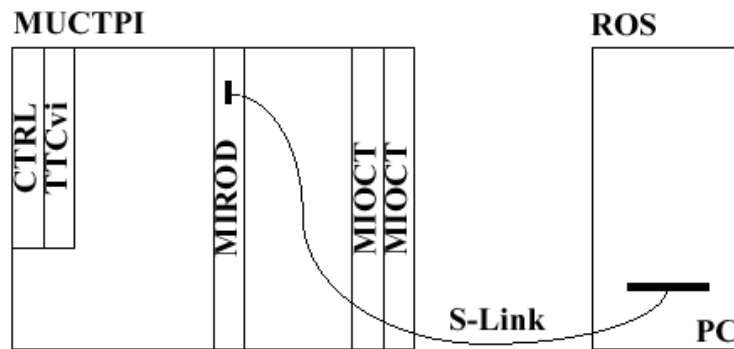
TTCvi – MICTP connections

Integration test of MUCTPI (2)

Done in 3,4/'01

- MUCTPI-ROS

- MIOCT,MIROD  ROS



ROS: (just for s-link dest.)
PC (Linux) with S-link
Destination Card

- S-link Test (Verification)
- Collapsed ROS:
TRG/EBIF/ROB tasks

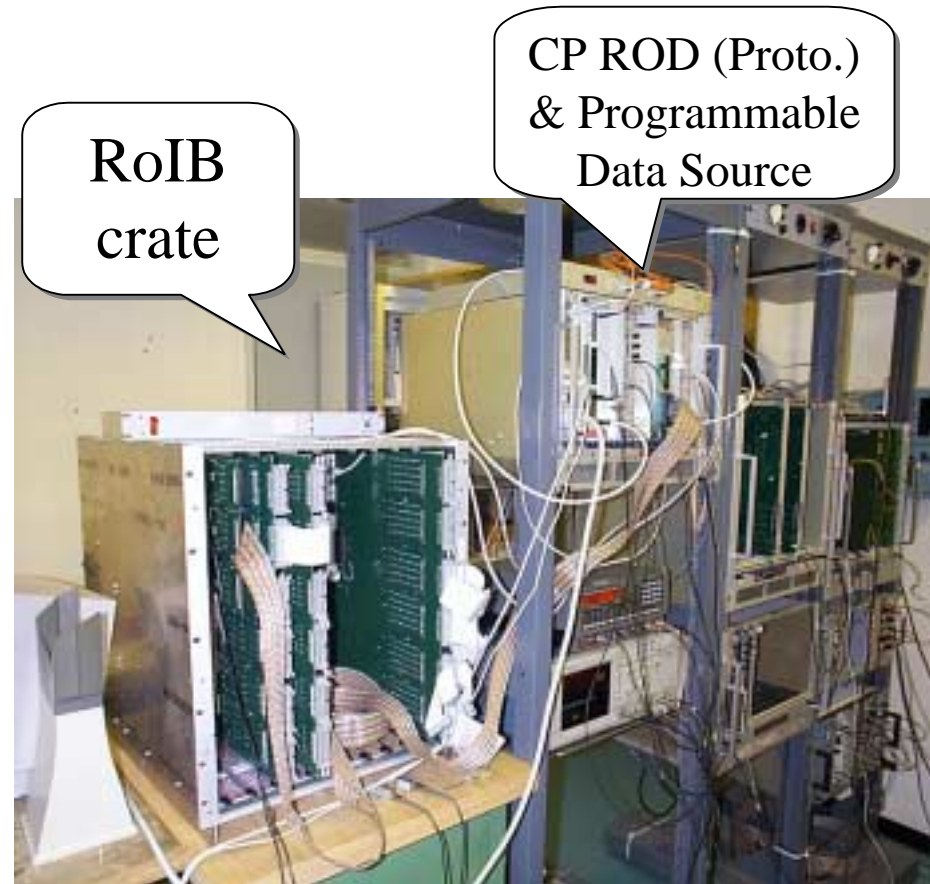
- Results

- MIOCT,MICTP,MIROD to ROD : 10 KHz with 14 μ cand., data OK
 - MIROD test memory to ROS (~30 μ cand.) :
 - 100 (75) KHz with simple s-link test with(out) data verification at ROS
 - 35 KHz with a combined TRG/EBIF/ROB task
 - Current ROS system limits the throughput. MIROD could send with 1MHz
 - **Depth and logic around DAQ FIFO in MIROD will be refined for the final implementation**

Integration of CP/JEP ROD with RoIB and ROS

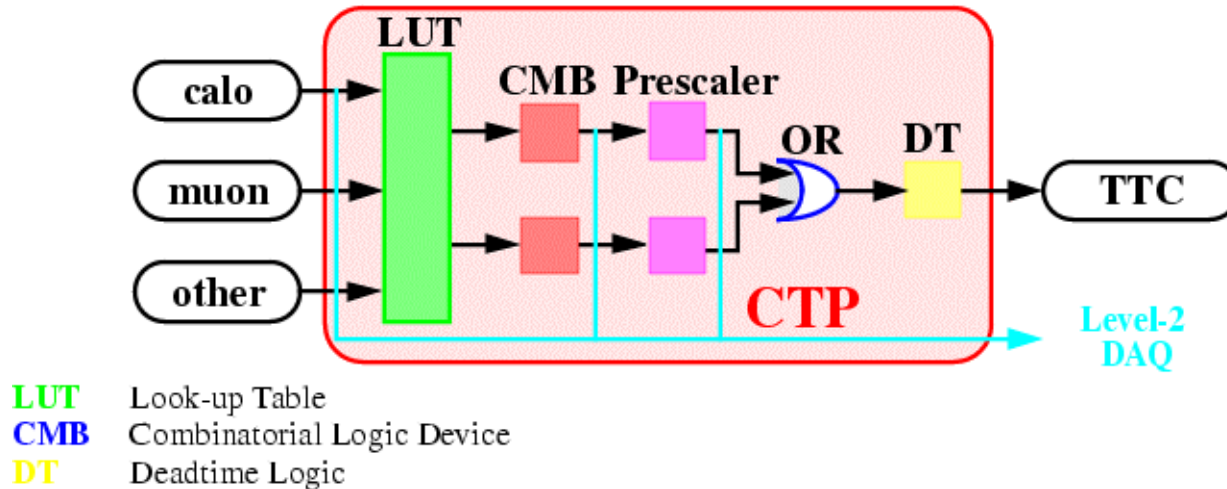
Done at CERN in 4/'01

- RoIB
 - CP ROD $\xleftrightarrow{\text{S-link}}$ RoIB
 - Data transfer with low frequency works fine
 - < 500 Hz sustainable with data verification
 - L1A at CP ROD to RoIB in was $\sim 2.25\mu\text{s}$
 - Data Transfer with Higher frequency has problems with
 - Data flow control
- ROS
 - Data transfer with 20 KHz
 - Data flow control problem



Problems will be identified and fixed before slice test in autumn 2001

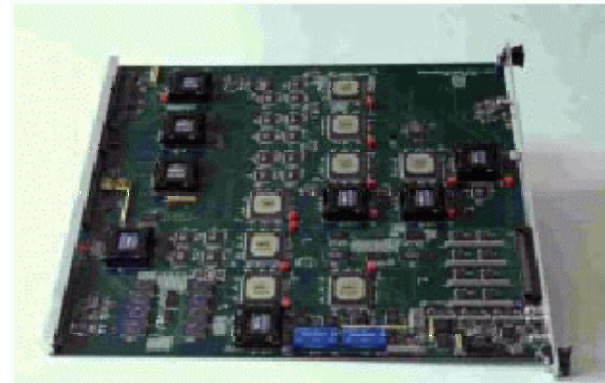
Central Trigger Processor (CTP)



- Trigger inputs (128 bit in TDR, now 160 bit) from calo, muon and others (cosmic, calibration)
 - Multiplicities (e/γ , $\tau/\text{had.}$, jet, μ), ΣE_T , E_{miss} etc.
- 96 items of Trigger menu, which are individually pre-scalable, can be constructed based on combinatorial logic system
- Level-1 decision with OR of all trigger items, sends L1A to TTC
- Adds dead time (DT) to prevent for FE electronics
 - Prevents overlapping read and buffer overflow

CTP status & plan

- CTP Demonstrator (32 inputs) implemented
 - Prototype will be used for integration tests with other parts of LVL1 and HLT/DAQ in 2001/2002
- PDR for final CTP done in 4/99
- Trigger Menu handler software developed in last year
- Detailed design of final CTP will be started soon in 2001
 - Increase of input 128 bit to 160 bit
- FDR will be in 3/2002



32 inputs CTP demonstrator prototype

LVL1 Status Summary

■ Calorimeter

- All main processors except PPr ASIC are now FPGAs
- First integration between CP/JEP ROD and RoIB,ROS has been done.
- PPM,CPM,JEM,CMM Full specification prototype being built in this summer
- Slice test starts this autumn

■ RPC (Muon Barrel)

- CM ASIC Place & Routing finished, Mask may be now completed. Submit in Sep., '01
- PAD,splitter box design completed, prototypes is being built
- Link Rx module at off detector part design started
- Slice test will be in 2002

■ TGC (Muon Endcap)

- Test of main 3 ASICs started, no major problem found.
- Prototype boards of Patch Panel+Slave, Service PP, Hi-pT,SL, ROD, SSW, HSC/CCI being built and testing
- Slice test starts this autumn

■ MUCTP/CTP

- Prototypes of all MUCTP modules built and tested except MICTP
- First integration with RoIB,ROS has been done
- Integration with RPC,TGC SLs will start later this year
- Final CTP module design will start soon
- Integration of MUCTP and CTP to be done later this year