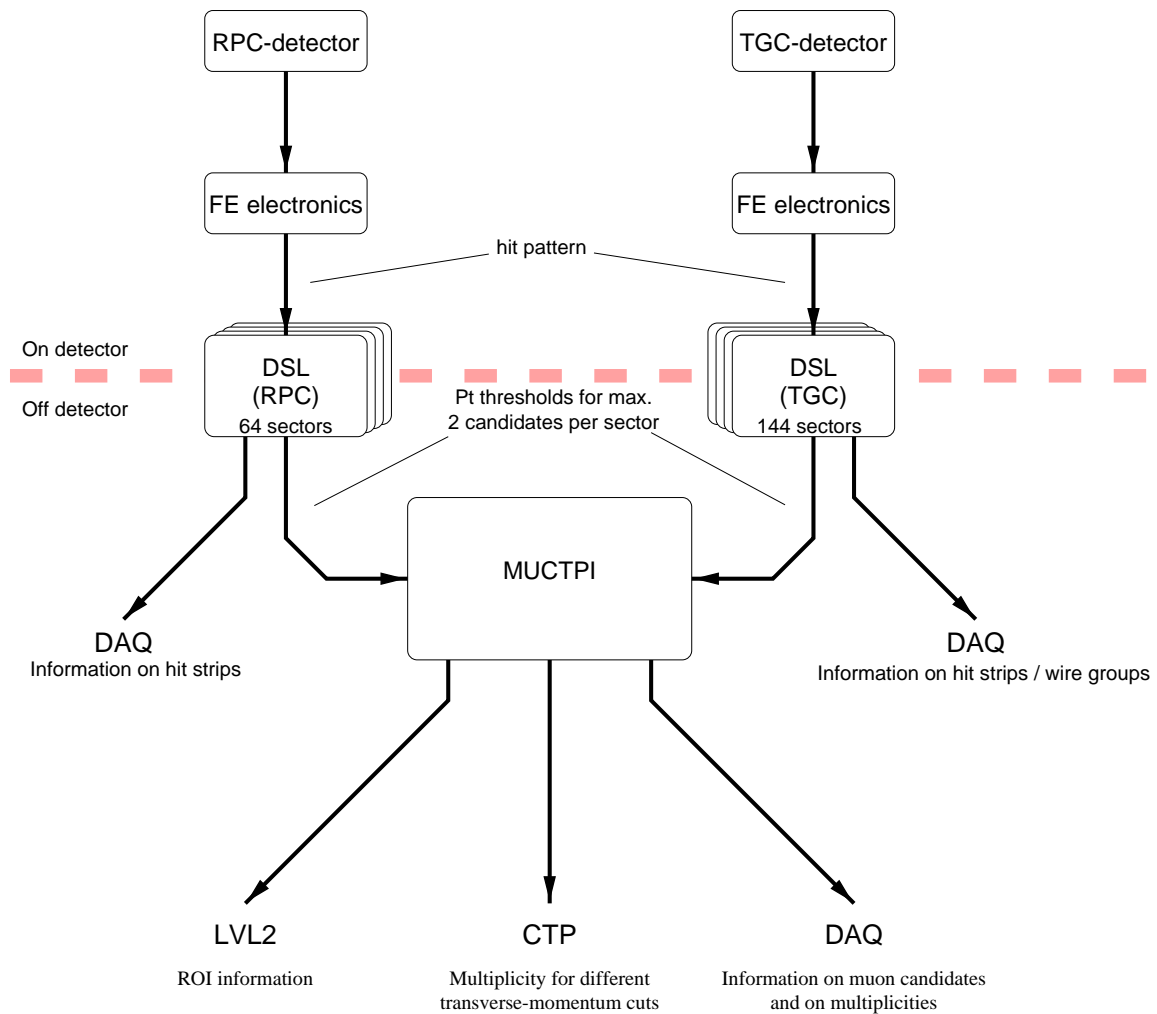


13 The muon trigger interface to the CTP

13.1 Introduction

As already discussed in Chapter 9, the muon trigger system is composed of three subsystems (see Figure 13-1) – detector-specific logic (DSL) associated with the RPC and TGC detector systems (see [13-1][13-2] for a detailed description of the TGC and RPC) and the muon trigger / CTP interface (MUCTPI). The DSL subsystems associated with the RPC and TGC



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Figure 13-1 Data flow in the muon-trigger system.

systems were described in detail in Chapters 11 and 12 respectively. References [13-3] and [13-4] summarize the trigger schemes for barrel and end-cap regions. This chapter describes the MUCTPI subsystem.

The results from the DSL that form the input to the MUCTPI provide information on up to two muon-track candidates per sector. The information includes the position and p_T range of the track candidates. The MUCTPI combines the information from all of the sectors and calculates total multiplicity values for each of the six p_T thresholds. These multiplicity values are sent to the CTP. Note that in forming the multiplicities care has to be taken to avoid double-counting single muons in regions where trigger chambers overlap. Otherwise doubly-counted single muons could dominate the low- p_T dimuon trigger, giving an unacceptably high rate.

Additional functions of the MUCTPI are to provide data to the LVL2 trigger and to the DAQ system for events selected at LVL1. The LVL2 trigger is sent a formatted copy of the information on candidate muon tracks. This information is used to define regions of interest (RoIs) that drive the LVL2 muon-trigger processing. The DAQ system receives a more complete set of information, including in addition the computed multiplicity values. The information sent to the LVL2 trigger is ordered, according to decreasing in p_T .

13.2 Summary of requirements

The MUCTPI collects data from the DSL; after data processing and formatting, results are sent to the central trigger processor (CTP), the LVL2 trigger, and the DAQ. A detailed list of the technical requirements for the MUCTPI can be found in Ref.s [13-5] and [13-6]. In the following, a short summary of some of the main requirements is given, as needed for the understanding of the systems implementation.

- Some muons cross overlapping trigger chambers in such a way that hits are produced in both chambers. If the chambers belong to different sectors, the DSL may send two muon candidates caused by the same particle to the MUCTPI. The MUCTPI must make sure that such candidates are counted only once. To do this it uses information indicating if a muon candidate has been found in a region where trigger chambers overlap.
- The DSL can send up to two muon candidates per sector to the MUCTPI. In order to allow for some flexibility in forming the LVL1 trigger decision, two methods of forming the multiplicities have to be provided: for each sector either all muon candidates are taken into account, or only the candidate with the highest p_T contributes to the multiplicity calculation. The two options have to be independently programmable for each of the six p_T -thresholds.
- The maximum overall multiplicity that needs to be handled by the system is seven candidates. Larger multiplicity values are rounded down to seven.
- For all data which are read out via the DAQ system, pipelines have to be implemented which hold data for a time corresponding to the latency of the LVL1 system. In addition it must be possible to read out data from a programmable window of up to ± 2 bunch-crossings (BCs) width around the LVL1 trigger. This is needed for setting up the timing of the system and also facilitates monitoring of activity in the trigger chambers shortly before and after the event which caused the trigger.
- Since the data received by the MUCTPI come from different parts of the detector the MUCTPI must align the incoming data in time, compensating for different times of flight and signal propagation delays, so that only data corresponding to the same bunch crossing are used to form multiplicities and for defining RoIs.

- The latency of the MUCTPI, measured from the arrival of the last piece of data from the DSL until the last piece of information has arrived at the CTP, must not exceed eight BCs.
- The interface to the LVL2 trigger must operate without data loss up to a LVL1 trigger rate of 100kHz. The latency for providing the trigger information to LVL2 should not exceed 100 μ s.
- The DAQ interface must cope with the maximal expected occupancy at full luminosity without losing data.
- Sufficient online monitoring information must be provided in order to check the correct functioning of the MUCTPI during beam running and to facilitate fast localization and diagnosis of possible problems.

13.3 Interfaces

The MUCTPI has interfaces to the DSL, the CTP, the LVL2 trigger and to a readout buffer (ROB) for the DAQ (see Figure 13-1). Other interfaces not shown in the figure are to the TTC system (provides clock and trigger signals), to the run-control system and the monitoring system, and to the DCS (for monitoring of power supplies and crate cooling).

13.3.1 Interface to DSL

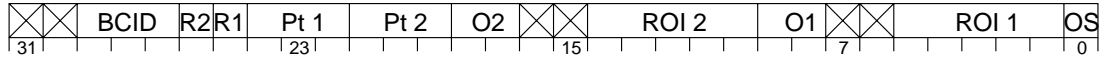
As discussed above, the DSL is divided into sectors readout each of which provides information to the MUCTPI. In total there are 208 sectors, 2×32 for the barrel, 2×48 for the end-caps and 2×24 for the forward regions. For each sector, one 32-bit word is received at the BC rate (40MHz). Figure 13-2 illustrates the detailed format of these words [13-7]. Each word contains information on up to two muon candidates. The p_T thresholds of the candidates are encoded with numbers from one to six. The location of each candidate in the sector is given by the RoI address. For the barrel and end-cap, flags indicate if the candidate was found in a zone of overlapping barrel sectors or of overlapping barrel and end-cap sectors. These flags are used to avoid double-counting muons in these zones when forming the total multiplicities. An overflow flag signals the presence of more than two candidates in a sector. Since the barrel DSL can handle at most one candidate in a group of four RoI regions (so-called pad), and the end-cap and forward DSL can handle only one candidate per subsector, additional overflow flags indicate if more than one candidate occurs in these regions. In all cases of an overflow, the highest p_T muon candidates are kept. Candidates within a sector are ordered according to p_T . Candidate 1 refers to the highest- p_T candidate and candidate 2 to the second-highest- p_T one.

The data words are received in the MUCTPI by 16 so-called octant boards which will be described below. Each board receives data from 13 sectors covering a full octant for one end of the detector.

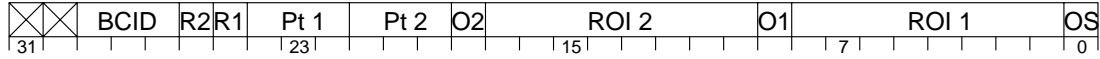
13.3.2 Interface to CTP

The connection from the MUCTPI to the CTP has to be as fast as possible to minimize the latency. Since the MUCTPI and the CTP will be located very close to each other in the same rack or in adjacent ones, the cable length is only of order a metre. The six 3-bit multiplicity values will be sent as differential electrical signals, for example using twist-and-flat cables.

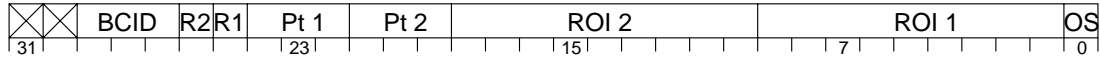
BARREL format:



ENDCAP format:



FORWARD format



- XX : reserved
- 1 : refers to the highest-pt candidate
- 2 : refers to second highest-pt candidate
- OS : more than 2 candidates in the sector
- ROI : ID of region of interest
- O : barrel : 01 overlap with neighbouring barrel sector
10 overlap with adjacent endcap sector
11 overlap with barrel and endcap
endcap : overlap with adjacent barrel sector
- Pt : transverse momentum threshold (1..6)
- R : more than 2 candidates in one pad
- BCID : lowest-order three bits of BCID

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Figure 13-2 Format of the input data coming from the DSL.

13.3.3 Interface to LVL2

Information on muon candidates must be sent to the LVL2 interface so that the LVL2 trigger processor can build up regions of interest which it then investigates closer using information from other subdetectors. For every event triggered by LVL1 the following information must be sent:

- The event number and the BCID number
- The number of muon candidates to be sent
- A flag indicating if not all found muon candidates could be sent to LVL2. [The total number of candidates sent to the LVL2 trigger will be limited to a fixed number.]
- For each muon candidate which is sent to LVL2:
 - a. The p_T range of the candidate.
 - b. The sector identifier and subsector address of the candidate.
 - c. A flag indicating if it was the highest- p_T or the second-highest- p_T candidate in its sector.
 - d. Flags indicating if the candidate was found in a region of overlapping sectors.

- e. Flags indicating if more than two candidates were found in the sector or more than one candidate in the subsector.

The physical implementation of the interface has not been finally decided. A possible solution which exists today is the S-LINK interface [13-8].

13.3.4 Interface to DAQ

For each event triggered by LVL1, the information that is sent to LVL2 is also sent to the DAQ system via a ROB. In contrast to LVL2, which receives the information only for the selected bunch crossing, the DAQ is sent information in a time frame of up to ± 2 BC around the triggered one. The DAQ receives as additional information, also in a time frame of up to ± 2 BC around the triggered one, the multiplicity values calculated by the MUCTPI.

As discussed in Section 13.4.4 below, the physical link to the DAQ will be the ATLAS standard readout link.

13.3.5 Interface to the TTC

The MUCTPI receives various standard signals from the TTC system: the LHC clock (BC) from which the local system clock is derived, the bunch-counter reset signal (BCR) used to check the synchronization of the readout, and the LVL1 trigger decision (L1A) used to initiate the readout for selected events.

13.4 Functional partitioning and specification

The MUCTPI is divided into a number of building blocks which are housed in one 9U VME crate shown in Figure 13-3. In addition to the modules drawn, there will be a VME master in the crate (e.g. commercial CPU module).

The different functionalities of the MUCTPI are implemented in three types of VME modules which are connected to each other via an active backplane. The functionality of the MUCTPI is shared by these system components as follows (see Figure 13-4):

- 16 so-called octant boards (MIOCTs) receive data corresponding to an octant in the azimuthal direction and half the detector in the η direction. They form muon-candidate multiplicities for this region, correctly taking into account the overlap zones between barrel and end-cap sectors. There is no overlap between muon trigger chambers associated to different octant boards.
- The Muon Interface to the CTP (MICTP) contains the driver unit to the CTP.
- The Muon Interface to Read Out Driver (MIROD) drives, after some data formatting, data to the ROI builder of the second-level trigger and serves as the interface to the Read Out Buffer (ROB).
- All modules are connected via the Muon Interface Backplane (MIBAK). It contains two components: The active part forms the total candidate multiplicities by adding the multiplicities of the MIOCT boards. The passive part contains a bus system to transfer data from the MIOCTs and the MICTP to the MIROD.

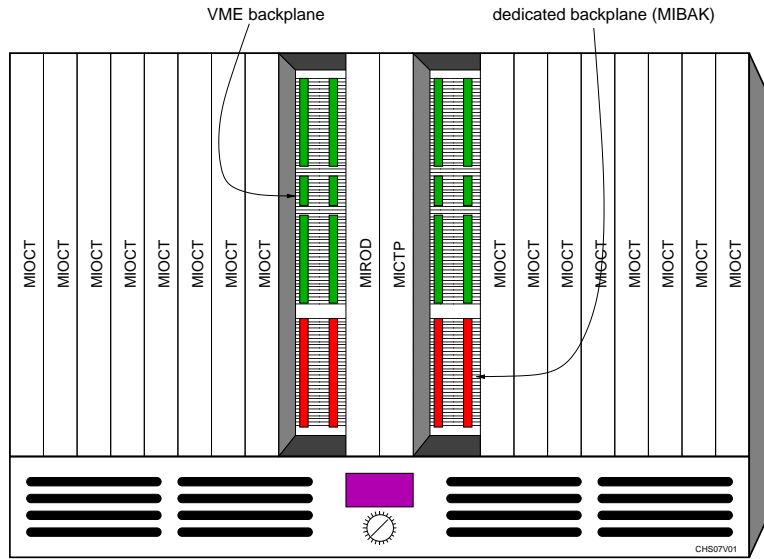


Figure 13-3 The layout of the MUCTPI crate.

13.4.1 The Octant boards

Sixteen Muon Interface Octant boards (MIOCTs) receive data from the DSL. The octant boards are divided into two groups which cover the positive and the negative rapidity regions of the detector. Each octant board receives data from four barrel, six end-cap, and three forward sectors. The region covered corresponds to one octant in azimuthal for half the detector.

Figure 13-5 shows the block diagram of one octant board. After signals are received from the DSL they are synchronized to the phase of the internal BC clock at the input of the MIOCT boards. Sampling is done on the positive or negative edge of the internal clock depending on the position of the input signal transition with respect to the internal clock. A TDC [13-9], incorporated in the octant board, is used to determine the appropriate sampling transition and, during running, to monitor in the timing of incoming signal transitions. Note that the variation in this timing is expected to be negligible because the timing is determined by properties of the interconnection cables and the fixed relative phase of the BC clock in the sector logic and the octant board.

After synchronization, the different input signals have to be aligned in time. This is necessary because of different processing latency between the RPC and TGC-based sector logic, and also because of different cable lengths and times of flight for different parts of the system. The alignment stage in the MIOCT boards is performed using configurable-length shift registers (range 0–10 BCs)¹. The right configuration for the length of the registers can be determined using test events sent by the DSL to the MUCTPI. The data word of each sector contains a bit field with the three least significant bits of the BC (see Fig. 13-2). The length of the shift registers

1. Note the distinction between programmable and configurable parameters. The former can be changed simply and rapidly through memory accesses. The latter are used for parameters that do not change once the system has been set up — they can be changed through relatively slow and complicated procedures, for example by loading new FPGA configuration files.

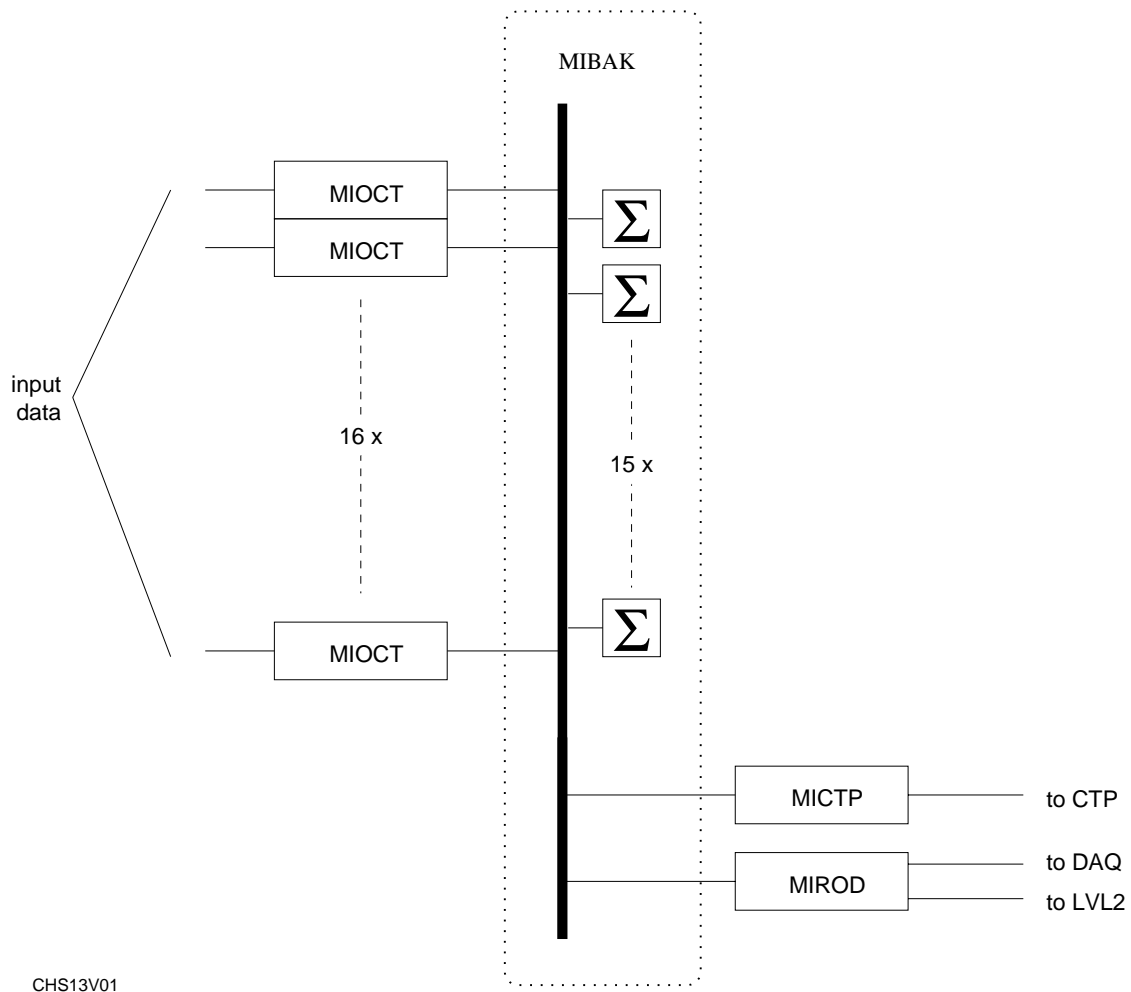
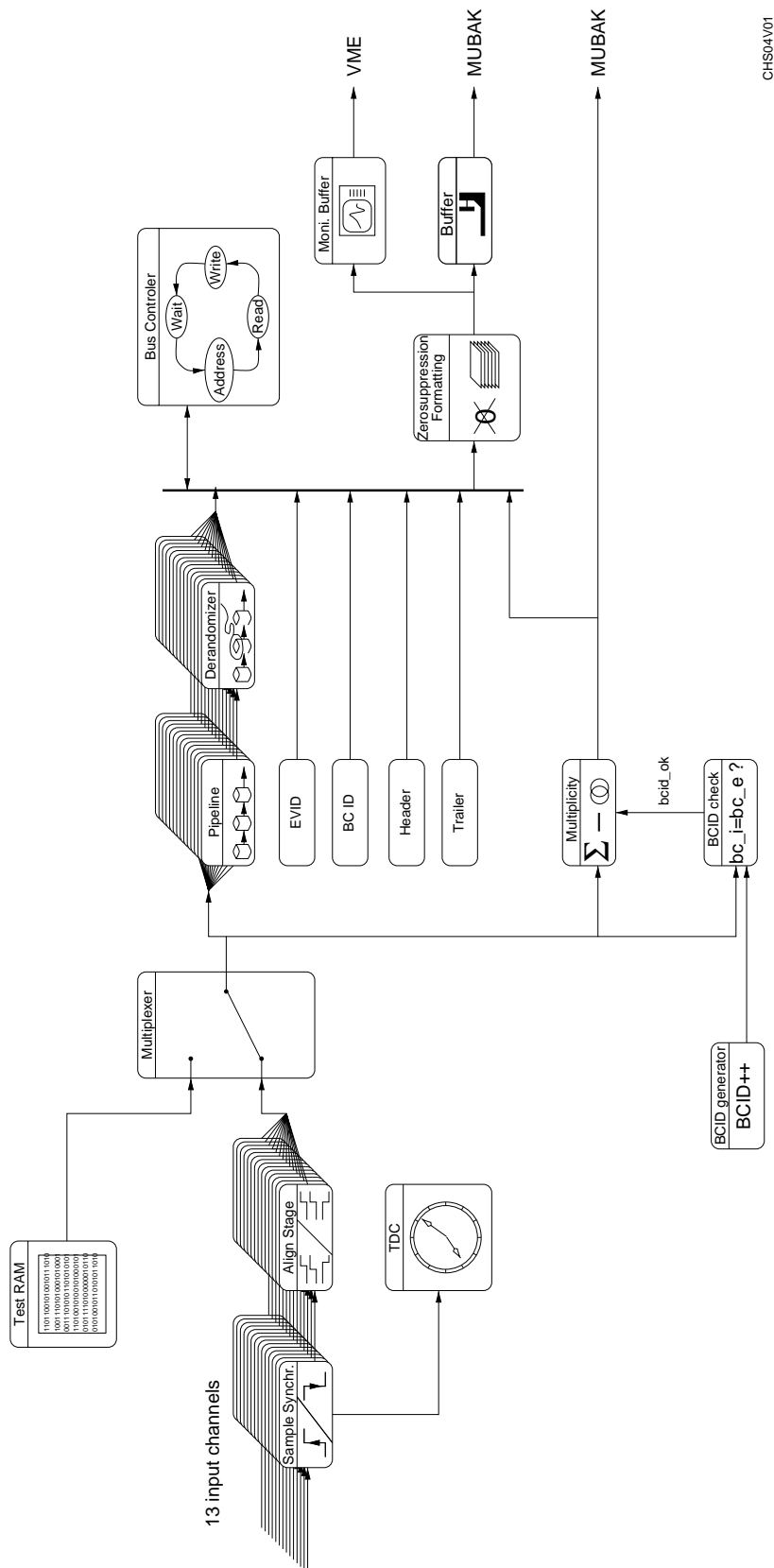


Figure 13-4 Functional partitioning of the MUCTPI.

has to be configured so that the BC numbers of all data words coming from the same L1A are equal.

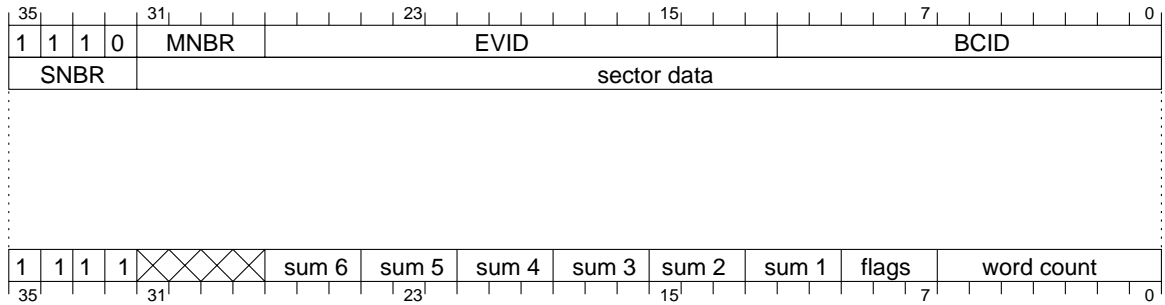
All the data received from the DSL are stored in pipeline memories for the duration of the latency of the LVL1 trigger. In case of a LVL1 Accept (L1A), data of all input channels have to be read out of the pipelines by the derandomizers and written into the local readout buffer. A programmable window around the triggered BC can be defined. Up to ± 2 bunch crossings around L1A can be read out. At a L1A rate of 75 kHz, the total data rate in an octant board is 176 Mbit/sec (13 input channels; 32-bit input word extended by 4-bit channel ID; maximum 5 BC long time frame; 75 kHz rate).

Before data of the 16 octant boards can be sent via the internal backplane to the MIROD, a zero-suppression stage is needed in order to reduce the data rate to a tolerable level. Subsequently, data belonging to one L1A are formatted into a data package (with header and trailer) and buffered until they are read out via the backplane. The data format of these packages is shown in Figure 13-6. The first word of every package forms a header containing a four-bit head-identification pattern (bits 31 to 35), the identification number of the MIOCT module (MNBR), the event number (EVID), and the BCID. What follows are one word for each sector containing



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Figure 13-5 Block diagram of the octant board.



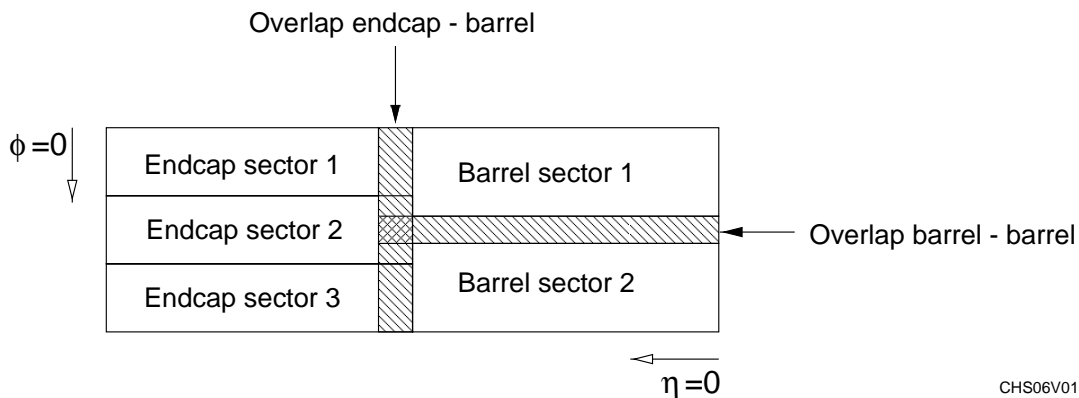
- MNBR : module number
- EVID : event number
- BCID : bunch crossing number
- SNBR : sector number
- sector data : information on muon candidates
- sum n : multiplicity per transverse momentum threshold n
- flags : various flags
- word count : number of words in one data frame

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Figure 13-6 Format of the data packages sent from the MIOCT modules to the MIROD via the backplane.

at least one muon candidate. The format of these words corresponds to the format of the input data to the MIOCT module (see Section 13.3.1). Additionally, the sector number (SNBR) is added in the four most significant bits. A trailer, identified by the pattern 1,1,1,1 in the four most significant bits, closes the data package. It contains the six multiplicity sums, three bits reserved for flags, and a word count indicating the total length of the data package in words.

The multiplicity logic counts the number of muon candidates for each BC clock in the six different transverse-momentum classes taking account of possible overlaps between adjacent barrel sectors and barrel and end-cap sectors. Figure 13-7 shows the position of these regions in



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Figure 13-7 Position of the overlap regions of the muon trigger chambers.

the muon trigger chambers. Each octant board covers two such structures. There is no overlap

between sectors associated to different octant boards. For each group of sectors corresponding to Figure 13-7, a fast truth table is used to detect the presence of muon candidates in different sectors which could be caused by the same particle. Figure 13-8 illustrates how the truth tables, together with a set of lookup tables, avoid the double counting of muon candidates in overlap regions. If the truth table detects two muon candidates in the same overlap region belonging to different sectors, it asserts a veto for one of the candidates. The subsequent adder stage will ignore candidates which have been vetoed. The outputs of all first-stage adders are summed to form six 3-bit sums which are clipped at a maximal count of seven.

In order to test the system without relying on data from the DSL, the input stage can be switched to a test RAM (256×32 bits) that can be loaded with an arbitrary test pattern via VME. Monitoring information is acquired from the system via its VME interface. In addition, VME is used to configure the FPGAs of the whole system. This allows for high flexibility even in the case when minor modifications are desired.

13.4.2 The interface board to the CTP

The interface board to the CTP, MICTP, collects the multiplicity sums for the six p_T thresholds over the custom backplane, MUBAK, described in Section 13.4.3 below, and transmits them to the CTP. The MICTP is responsible also for distributing time-critical control signals to the rest of the MUCTPI system.

13.4.2.1 Multiplicity formation for the CTP

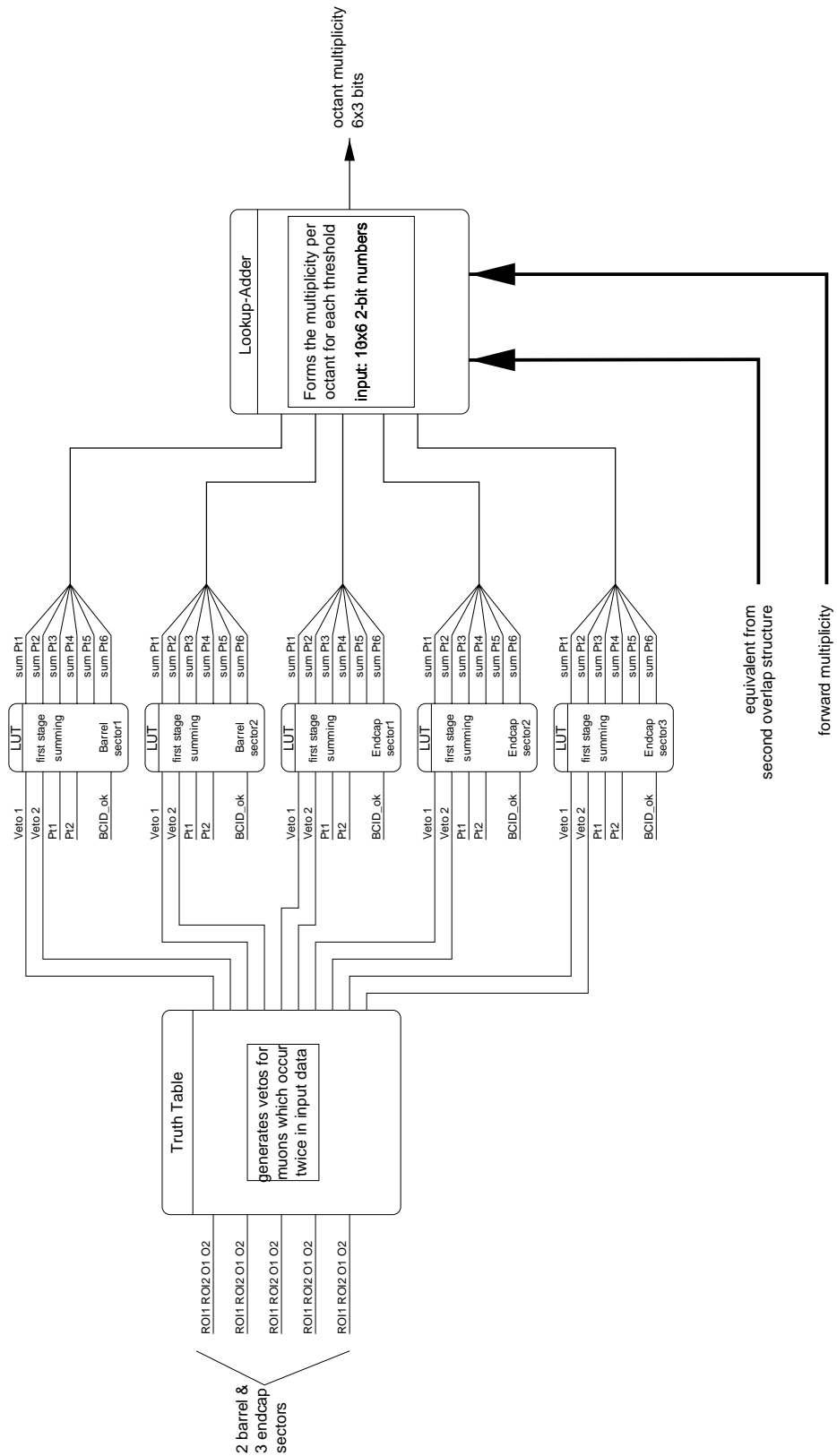
Figure 13-9 shows a block diagram of the MICTP. The upper part shows the building blocks receiving the total muon multiplicities from the MIBAK backplane; these are then driven to the CTP. In order to be able to test the CTP without relying on data from the MIOCT boards, the MICTP contains a programmable test-pattern RAM which can be multiplexed to the output drivers. Additionally a synchronization pattern can be driven to the CTP. This is used by the CTP to synchronize the input signals to the internal system clock.

The multiplicity sums that are sent to the CTP are also stored in a pipeline memory. In case of a LVL1 trigger, data from the pipeline are stored in a derandomizer. These data are subsequently read out by the MIROD module (see Section 13.4.4) over a custom bus on the backplane.

For monitoring purposes, eight counters for each p_T threshold count the occurrences of 0, 1, 2, ..., 7 muon candidates per bunch crossing. At the end of each LHC turn the contents of these counters are copied into a set of registers which can then be read via VME. At the same time the counters are reset.

13.4.2.2 Distribution of LVL1 control signals

The MICTP distributes the system clock to the rest of the MUCTPI. Under normal operation this clock is the LHC BC clock. For test purposes, an internally-generated 40 MHz clock can be used instead. Five other time-critical control signals are sent to all modules of the system via the backplane: The signals ECR (event counter reset) and BCR (bunch counter reset) reset all local event and bunch counters. The L1A signal is distributed to all modules to indicate a valid LVL1 trigger; this signal initiates the transfer of data from the pipelines to the derandomizers. The signal labelled 'synch moni' is used to synchronize the writing of monitoring information into



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Figure 13-8 Logic performing the sum of muon candidates within an octant board.

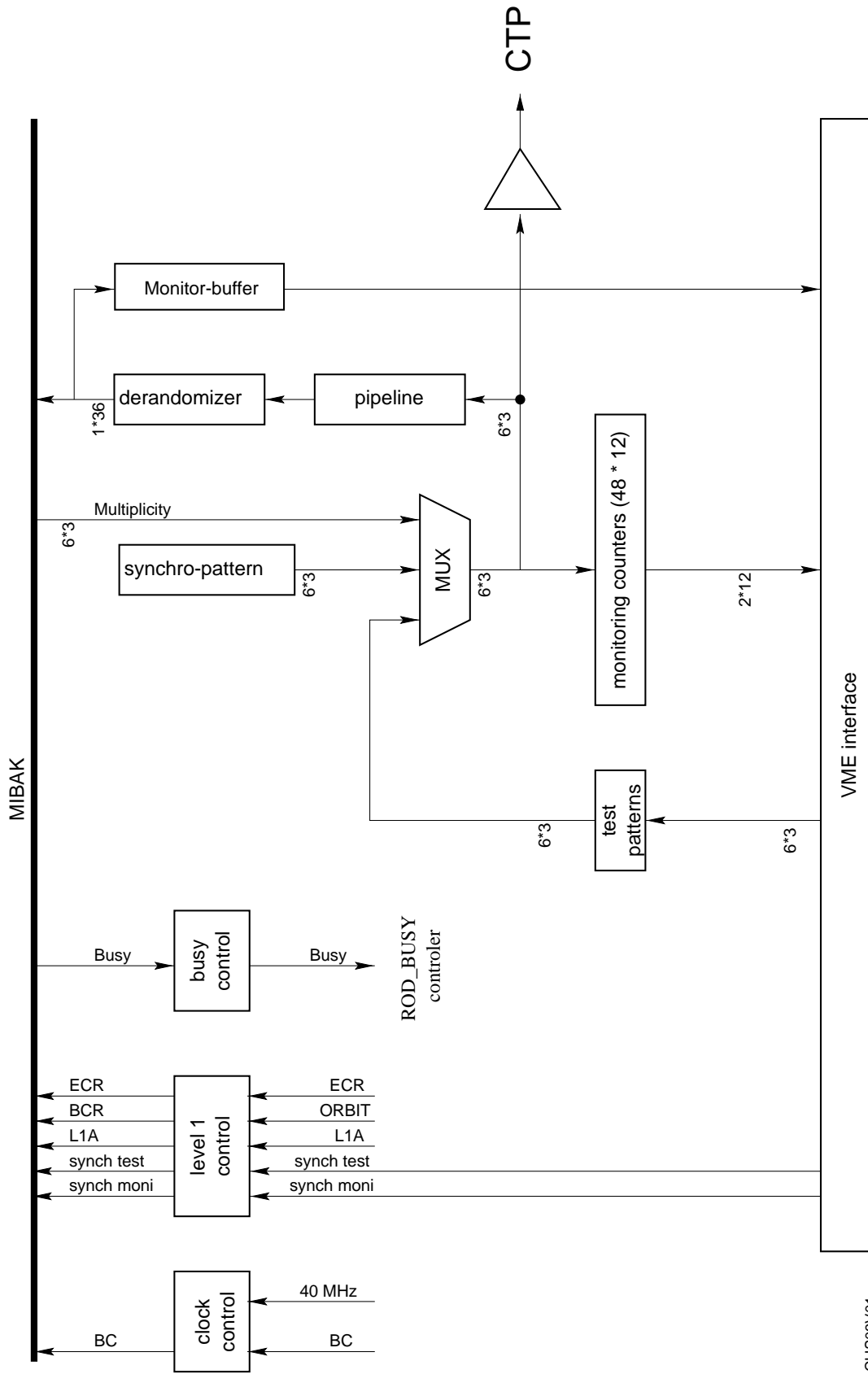


Figure 13-9 Block diagram of the MICTP.

dedicated buffers among all modules of the system, making it possible to investigate data belonging to the same L1A in all modules of the MUCTPI by reading out via VME the dedicated buffers. The signal 'synch test' is used to synchronously initiate the test cycle in which the octant boards are fed by the local test-pattern RAM.

In addition the MICTP monitors the BUSY line on the MIBAK backplane. Modules of the MUCTPI can activate this line in case they cannot accept more L1A triggers because their internal buffers are nearly full. In case of an activated BUSY in the system, the MICTP drives a BUSY signal to the BUSY_ROD module, which handles all BUSY signals generated in ATLAS (see Chapter 20).

13.4.3 The backplane

The backplane of the system consists of two parts. The upper part (J1, J2, J0) is a standard VME backplane. The lower part (J3), called MIBAK, is a custom backplane designed to form multiplicity sums over the MIOCTs, to move data from the MIOCTs and the MICTP to the MIROD, and to distribute time-critical signals in the system.

The octant boards are arranged in the MUCTPI crate as shown in Figure 13-3. Each octant board drives six 3-bit sums corresponding to the six different transverse-momentum thresholds onto the backplane. Additional summers are installed on the backplane itself, and connected as shown in Figure 13-10. It is possible to form the sums over the full detector in four layers of adders. The final results are received by the MICTP. The advantage of such an arrangement with respect to a solution where all active components are placed into the octant boards, is that signals have to traverse a minimum number of connectors. This leads to small signal distortions and minimizes propagation delays. Additionally the number of pins of the backplane connectors are minimized. In principle also an analog variant, in order to form the sums on the backplane, could be considered. After evaluating the times which would be necessary for digital-to-analog conversions before summing and analog-to-digital conversion of the results, no reduction of the system latency with respect to the digital solution can be expected. The digital version is preferred since it is less prone to noise on the backplane and therefore easier to implement.

In order to transfer data from the MIOCTs and the MICTP to the MIROD, a simple one-directional bus with high data throughput based on a token architecture has been developed. It is implemented in ECL technology in order to reach high readout rates at high data security. The bus is 36 bits wide in order to transfer the data packages described in Section 13.4.1. A simple handshake facilitates fast readout of all MIOCT buffers, as described in more detail in Section 13.4.4.

The MIBAK is used to distribute time-critical control signals to the MUCTPI system. The backplane layout must make sure that these signals arrive at all relevant modules of the MUCTPI crate with a fixed phase with respect to the BC signal. This ensures that in all modules these signals are synchronized to the same bunch-crossing.

13.4.4 The interface board to the LVL2 trigger and to the DAQ

Figure 13-11 shows a block diagram of the interface board to the LVL2 trigger and to the DAQ (MIROD). The MIROD module has to collect data from the octant boards and the MICTP before

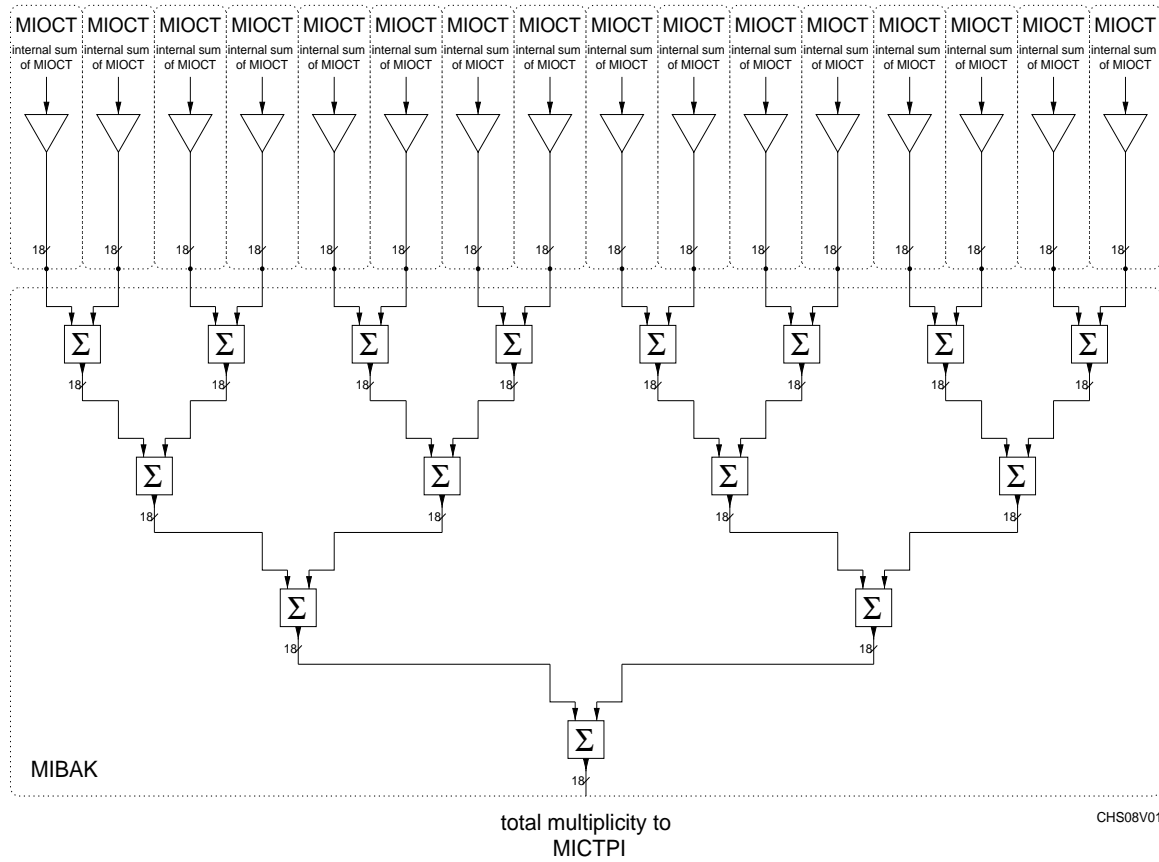
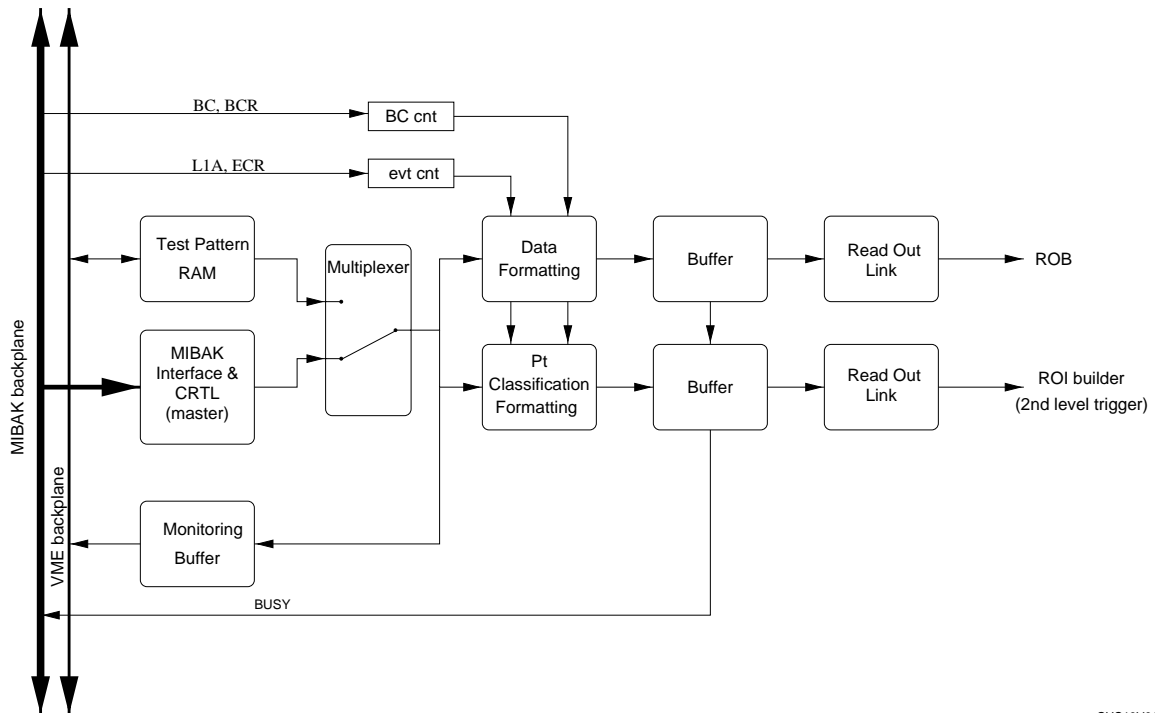


Figure 13-10 Schematic view of the part of the MUCTPI backplane which serves to form digital multiplicity sums among the octant boards.

sending them to the region of interest builder of the LVL2 trigger and the ROB of the DAQ system. The data are transferred over the token-ring bus implemented on the MIBAK. The bus is unidirectional and the MIROD module is the master for all transfers. After a L1A signal all slave modules have to indicate with a dedicated line on the bus that their data are ready for readout. The lines of all slave modules are combined in an OR. The MIROD module initiates a readout cycle as soon as all slave modules have their data available. It puts the token on the token ring which initiates the readout of the first module in the token-ring chain. The token subsequently propagates through all slave modules and returns to the MIROD module after the last slave has been read out. The synchronous readout works at a frequency of 40 MHz.

In order to provide the LVL2 trigger with the information necessary to form the RoIs, data received from the MIOCT modules on all muon candidates are classified according to their transverse momentum and then written into an intermediate buffer. The data used by the LVL2 trigger for the RoI generation belong to a single BCID. Within the window of data which is sent to the DAQ, the time slice for the data sent to LVL2 can be programmed in the MIROD.

In the MIROD, a p_T threshold can be programmed so that only muons exceeding this threshold will be sent to LVL2. In addition, it is possible to optionally take into account only the highest- p_T muon candidate of each sector. The total number of muon candidates transferred is limited to a fixed number (10 in the present design). A flag indicates if, due to this limit, not all candidates



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Figure 13-11 Block diagram of the MIROD.

are transferred. Candidates are ordered according to p_T before they are sent, the highest- p_T ones being sent first.

The MIROD module performs checks regarding the consistency of the data packages received from the backplane. For example, a check is made that all data sent for a given L1A come from the same BC. In case of inconsistency, the data sent to the ROB are flagged.

The MIROD module constantly monitors the status of its internal buffers. It asserts a busy signal in order to inhibit the generation of more triggers, which could lead to data loss, in case a buffer fills up close to its capacity.

In order to facilitate the monitoring of data arriving in the module, a buffer is filled with part of the incoming data. With help of a dedicated signal on the backplane, the filling of this buffer can be synchronized to the filling of equivalent buffers in the MIOCT boards. To be able to test the LVL2 trigger system and the DAQ system from the MIROD onwards, it is possible to feed the MIROD with test-data from a programmable RAM.

A prototype implementation for the links to LVL2 and to the ROB is the S-LINK [13-8]. It allows the transfer of data at a rate of 1.28 GBit/sec (32 bits at 40 MHz).

13.5 Overall latency calculation

The MUCTPI is designed such that it will not contribute more than eight BCs to the overall latency of the LVL1 trigger system. Figure 13-12 shows how the MUCTPI system components

contribute to that latency. The latency estimates have been done on the basis of electronics components which are on the market today.

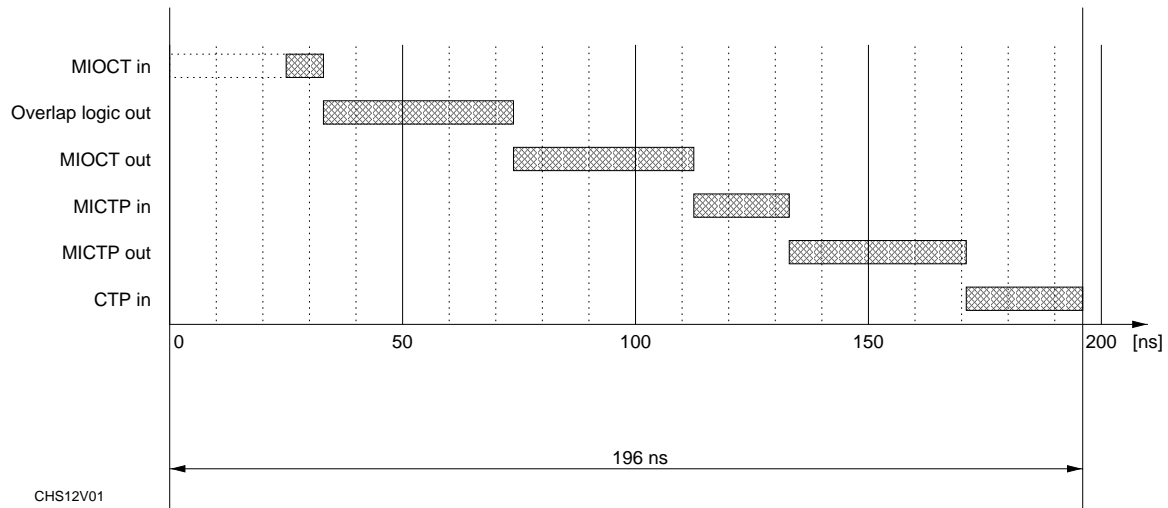


Figure 13-12 Breakdown of the latency contributions for the MUCTPI system components.

13.6 Summary of monitoring and test facilities

Important aspects of monitoring and testing have been pursued in the design of the MUCTPI system:

- By providing all modules with test-pattern memory it is possible to test every module independently of other hardware in the trigger system.
- By providing all modules with monitoring buffers, which are filled with data from the internal data flow and can be read via VME, it is possible to check the data coherence by comparing data read from the buffer with results computed from the input data. Additionally this information will be read out continuously during running conditions by the monitoring software. Histograms like, for example, hit maps and rate histories will be provided in order to monitor the correct functioning of the system.
- By providing a method to write synchronously in all modules to the monitoring buffers data of the same event, it is possible to trace data from the input to the output of the MUCTPI and compare the activity of the MUCTPI with expectations.
- Statistics on the formed multiplicities are provided by a set of counters in the MICTP for each LHC turn.

In order to make use of these online monitoring facilities, the MUCTPI contains a real-time VME controller. Efficient software is needed to read out the monitoring information while evaluating it and presenting it to the operators, so that possible problems in the system can be tracked down quickly.

More online monitoring is provided by the LVL2 and event-filter systems where the information of the MUCTPI can be combined with data from other detector components like for

example the muon precision chambers. These systems will be able to calculate online trigger efficiencies or noise levels in the muon trigger system.

13.7 Prototyping plans

A demonstrator programme is in process for the MUCTPI. A small prototype system will be built containing a MUCTPI crate with at least two MIOCT boards, a MIBAK backplane, a MIROD, and a MICTP board. At least two MIOCT boards are necessary in order to test the multiplicity formation via the backplane. The demonstrator prototype modules deviate from the final versions of the modules in the following respects:

- The MIOCT board has only one physical input for one sector. This is not a severe restriction for the demonstrator since arbitrary test patterns can be loaded in the test RAMs for the other sectors, and the hardware can be tested without restrictions using these test patterns.
- The signal receiver of the MIOCT board is implemented on a small mezzanine card. This allows different technologies to be tried out for the interface to the DSL.
- The overlap logic in the MIOCT module is implemented such that it ignores both muons of an end-cap sector if both of them overlap with the same barrel sector. This means that in these very rare cases the calculated multiplicity will be one too low. A modification of the truth tables handling the overlap will overcome this problem in the final version of the module.
- In the demonstrator MIOCT board, there is no memory foreseen in order to capture incoming data and read them out for monitoring purposes ([13-5]).

13.8 Construction and schedule

The MUCTPI components will be implemented using standard programmable logic components like FPGAs and CPLDs. The whole system can be built using technology available today.

Figure 13-13 shows the time schedule for the development of the MUCTPI. It is foreseen to have a minimal system consisting of at least two octant boards, a backplane, a MICTP, and a MIROD available end of 1999 so that the whole system can be tested in a test beam scheduled then. Afterwards possible changes can be implemented and the final system will be in production. A second test beam in 2002 is used to test the complete system. If necessary, after the test beam there is one more year available to implement modifications. The complete system will be available in the beginning of 2004.

13.9 Quality assurance and review procedures

A set of procedures and rules must be followed to assure the required quality of the system.

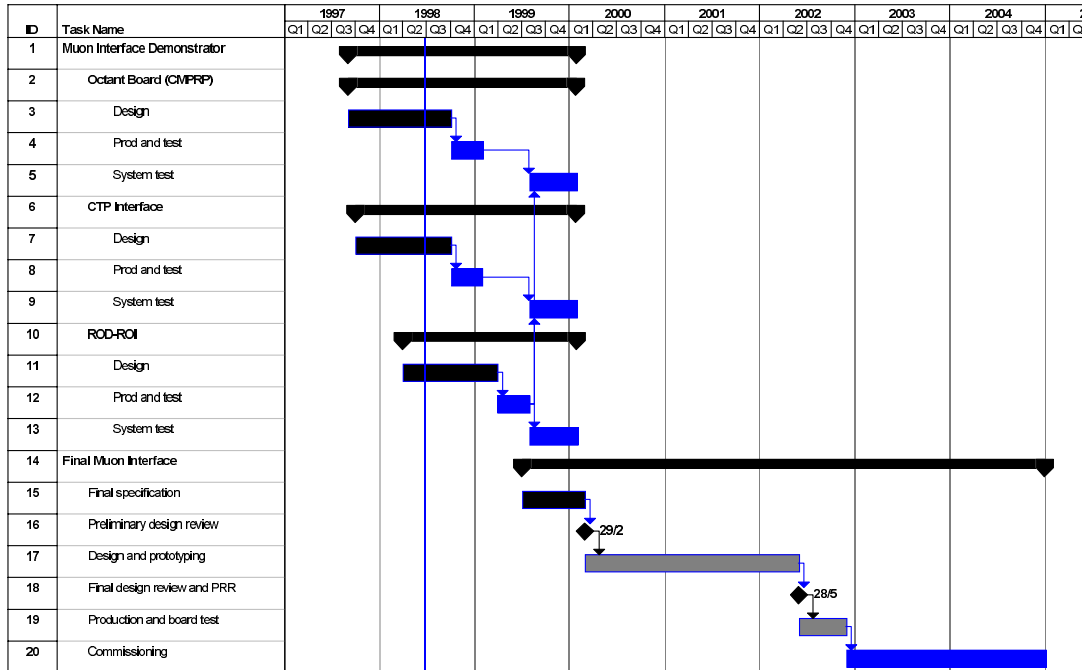


Figure 13-13 Time schedule for the MUCTPI.

The design and specification of each element will be subject to at least two review exercises — a Preliminary Design Review (PDR) and a Final Design Review (FDR) — with the possibility of an Interim Design Review (IDR) between them.

The PDR will be used to examine and assess the full requirements and specifications for the subsystem element, to identify any missing functionality, to ensure full compatibility with all connecting subsystems and to determine overall feasibility. This is perhaps the most important part of the review procedure, as it will determine the direction of subsequent engineering effort. Detailed written specifications will be supplied to the review group two weeks in advance of the review itself, and following the review the final agreed conclusions will be distributed to the level-1 muon trigger community.

IDRs may be held at any time during the design phase, but most usefully at the completion of schematic capture when many engineering issues (timing margins, interfaces to other subsystems, detailed latency calculations, etc.) can be explored. By monitoring progress at this stage some potential problems may be detected and resolved early, thereby minimizing wasted effort.

The FDR will be held before the MUCTPI design is sent for manufacture, and is intended to catch any design or engineering errors before budgetary commitment. This review will necessarily be of a more technical nature than the initial review, but there should be few problems to detect by this stage. It will be merged with the ATLAS production readiness review (PRR).

This review work has already been done for the prototyping. A user requirement document (URD) for the LVL1 muon trigger system has been written [13-5] and reviewed a first time by representatives of each subsystem.

Prototypes of each element will exist and be tested in the coming year. During that time, the final specifications will be written. The PRR will review them as well as the performance and functionality of the prototype system.

The construction of the MUCTPI components will follow usual rules, namely:

- Electrical tests of the PCB before assembly.
- Burn in of the boards after assembly by leaving them under power without cooling for two days.
- Test of the full boards.

Each element will receive a serial number and a database will be set up to store the information relative to each board: origin of the components which populate the board, results of tests, history of failure and location.

13.10 References

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- 13-5 *LVL1 Muon Trigger User Requirements Document (Draft version 1.4)*, ATLAS working document, ATL-DA-ES-0002, March 1998.
- 13-6 *Trigger and DAQ Interfaces with Front-End Systems: Requirement Document (version 2.0)*, ATLAS note DAQ-NO-103, June 1998.
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- 13-7 P. Farthouat, *Current Understanding of the Muon LVL1 System*, version 2, ATLAS note DAQ-No-89, May 1998.
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