

19 Strategy for setting up the timing of the experiment

19.1 Introduction

Several hundred thousand readout elements receive timing (BC clock), trigger (L1A), synchronization (BCR) and test (Test-pulse) signals. The phases of all these signals have to be adjusted in order to sample the input signals optimally, read out the proper event and maintain a coherent BCID number and hence synchronization over the whole experiment. There will be a very large number of delay elements to be adjusted and monitored, most of which are in inaccessible places, and these two tasks may require a lot of time.

Maintaining synchronization across a big experiment is always an issue even when the time between bunch crossings is large and the trigger rate is low (for instance in LEP experiments). In the case of the LHC, where the bunch-crossing period is very short, the trigger rate is very high and the number of detector channels is very large, making sure that all of the subdetector systems read out the same bunch crossing when a trigger occurs is a major issue.

In view of the above, the timing set-up is seen as critical and some automatic procedures must be defined to set up the timing for various modes of operation:

- beam-beam collisions;
- beam-halo triggers;
- cosmic-ray triggers;
- running with test pulses for test or calibration purposes.

Using the TTC system, the following timings have to be adjusted:

- BC clock phase at the front-end level (to ensure optimal sampling of the input signal);
- L1A arrival time at the front-end level (to ensure readout of the correct bunch crossing);
- Bunch Counter Reset (BCR) arrival time (to ensure a coherent BCID across experiment);
- test-pulse phase (test or calibration signal produced at the right time relative to the clock and the trigger).

Each subsystem must define a procedure to make these adjustments and this work is in progress in ATLAS. In this chapter, possible strategies are presented and discussed in general terms. In due course, each subdetector group will produce their own procedure which will be documented and formally reviewed.

This chapter presents example procedures for the following:

- timing set-up using beam for two representative front-end configurations;
- using test-pulses to make the timing set-up for beam;
- timing set-up for calibration with test-pulses.

The procedures for setting up the timing for cosmic-ray triggers and for beam-halo triggers have not yet been worked out in detail.

19.2 Timing set-up with beam

This section describes a possible automatic way to set up and check the coarse timing (i.e. everything except the fine BC clock phase adjustment) of the detector with beam. This can be applied only when beam is available; the next section will show that it is also possible to set up the timing with test-pulses, which will be of considerable interest during the commissioning phase of the experiment.

It is planned to make use of the LHC bunch structure and of the BCID values provided by the front-end electronics (FE_BCID), or the level-1 trigger electronics (BCID) as specified in Ref. [19-1]. Two cases are considered: in the first one the FE_BCID is formed before the level-1 pipeline and in the second one FE_BCID is formed after the level-1 pipeline. These two cases cover the vast majority of the ATLAS front-end systems.

The fine BC clock phase adjustment procedure is subdetector-dependent and can be done either before or after the coarse timing has been done (e.g. by looking at distributions of pulse-peak position or number of hits versus time). In the latter case, an iteration on the coarse alignment procedure might be necessary.

19.2.1 FE_BCID formed before the level-1 pipeline

Figure 19-1 shows a simplified block diagram of the front-end electronics circuitry when the FE_BCID value is formed before the LVL1 pipeline.

The timing and trigger signals are transmitted to geographical regions of the subdetectors which house a large number of channels, and within which there is no need for fine timing adjustment. For instance in the TRT, such a region is 1/32 of a wheel in the end-cap, which corresponds to 200–400 channels depending on the type of wheel; in the liquid-argon calorimeter a region corresponds to a front-end board which houses 128 channels.

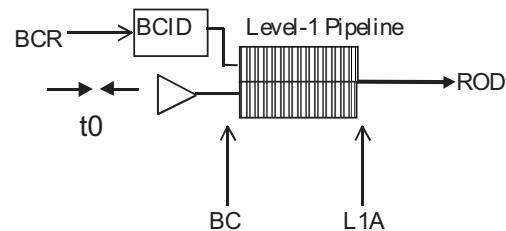


Figure 19-1 Block diagram of the front-end element with the BCID formed at the input of the level-1 pipeline.

Figure 19-2 shows a flow chart of the timing adjustment procedure. This procedure is organized in two steps.

In the first step, random L1A signals are generated and data are read out. For each timing geographical region, a histogram is built of the number of hits (in the sense of the presence of a signal above threshold) versus the FE_BCID received from the front-end. This histogram should reflect the LHC bunch structure, but be shifted in time as shown in Figure 19-3. The BCR timing is then adjusted in order to get FE_BCID = 1 at the correct place.

In the second step, the system is run with L1A fixed at BCID = 1. The event readout will generally give a FE_BCID value not equal to 1 since the L1A timing has not yet been adjusted. The L1A timing is then adjusted in order to get the correct FE_BCID value.

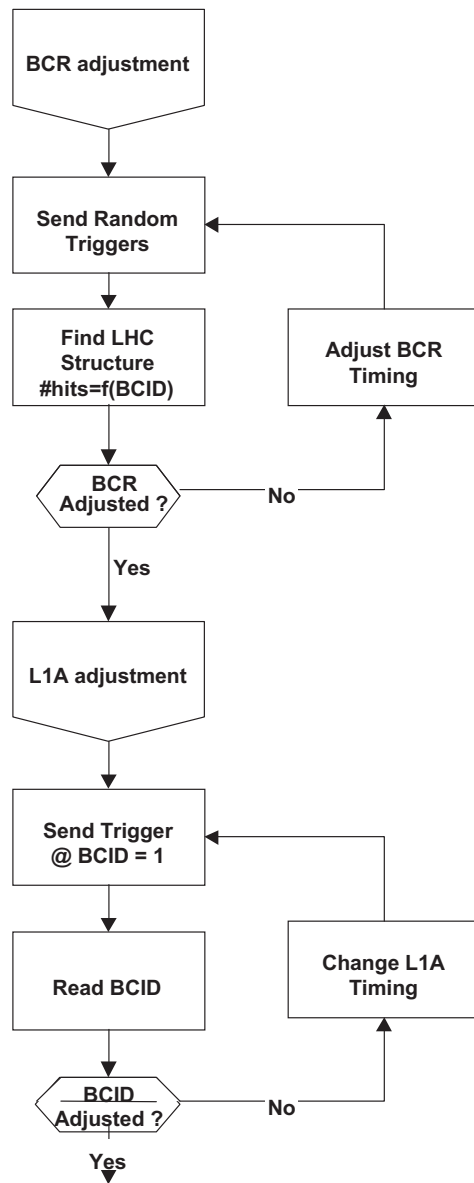


Figure 19-2 Simplified flow chart of the timing set-up with beam when FE_BCID is formed before the level-1 pipeline.

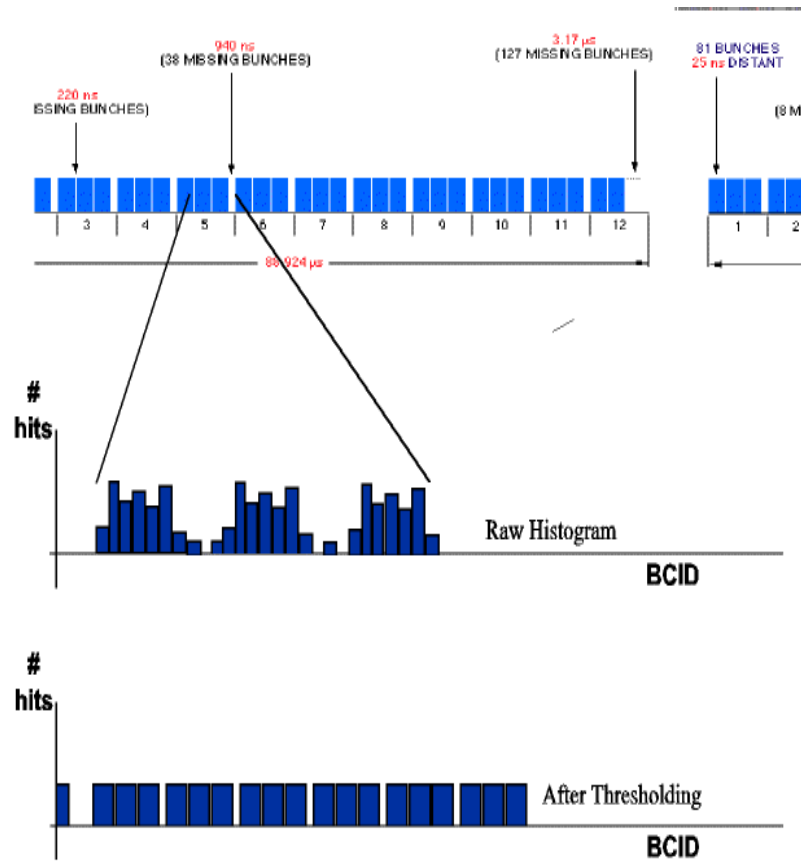


Figure 19-3 Hits versus BCID.

19.2.2 FE_BCID formed after the level-1 pipeline

In some front-end systems, the BCID number is formed after the Level-1 pipeline, when the L1A occurs (as shown in Figure 19-4). In this case, if one has bad timing of the L1A and BCR signals, the FE_BCID value will be wrong and equal to $FE_BCID_{true} + Error_{L1A} + Error_{BCR}$. Here the procedure described above in Section 19.2.1 has to be modified slightly, as shown in Figure 19-5.

In the first step, L1A signals are generated for each value of BCID and data are read out. For each geographical region, the histogram of the number of hits (sum of all the channels in the zone) versus the expected BCID number is built. This histogram should reflect the LHC bunch structure, but be shifted in time as shown in Figure 19-3. This histogram has to be shifted in one or other direction by a number of bunch crossings to coincide with the LHC bunch structure. The L1A signal delay is adjusted by this number of clock cycles. It has to be noted that until the fine BC clock phase adjustment has been done, an error of plus or minus one BC can be present.

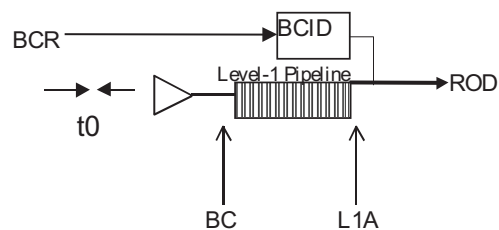


Figure 19-4 Block diagram of the front-end element with the BCID formed at the output of the level-1 pipeline.

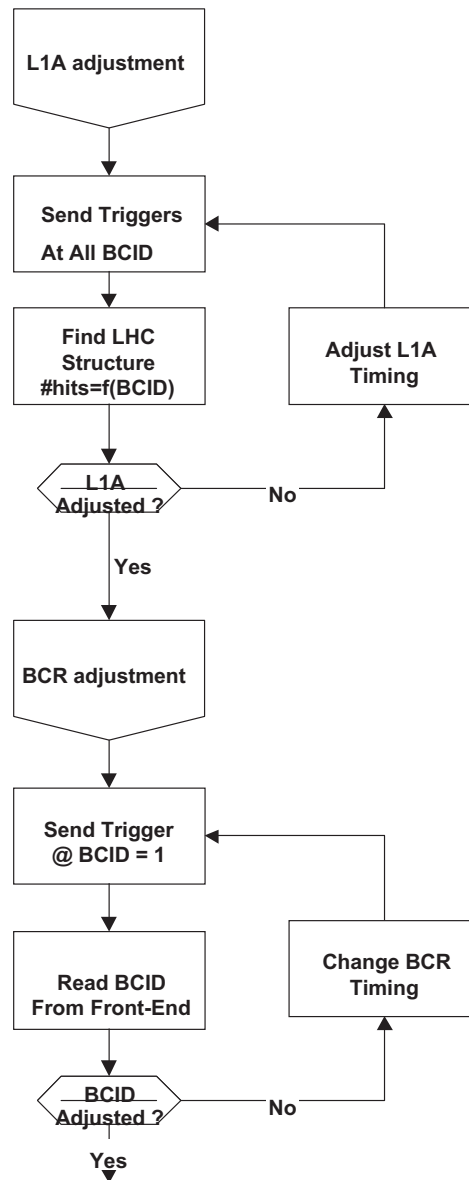


Figure 19-5 Simplified flow chart of the timing set-up with beam when the FE_BCID is formed after the level-1 pipeline.

In the second step, the system will be run with L1A fixed at BCID=1. The event readout will generally contain a FE_BCID different from 1 since the BCR signal timing has not yet been adjusted. The BCR delay is then adjusted in order to obtain the correct FE_BCID value from the front-end.

This method can be implemented very efficiently at high luminosity as the time needed to build the histograms will be very short. It can also be used to check the timing alignment at the beginning of a run for instance.

At low luminosity, the occupancy of the different subdetectors may not be sufficient to use this method efficiently, and, obviously, in the absence of beam this technique cannot be used.

19.3 Timing set-up for beam using test-pulses

It is extremely useful to be able to set up the timing ready for beam before the beam is available. Two objectives are being pursued:

- Set up the timing of the different parts of a subdetector so that only a single global adjustment is needed to align it in time with the other subdetectors.
- Set up the timing of each subdetector with respect to the others. This could be used during the commissioning phase of the detector to have as complete as possible data-taking tests.

This section shows that, at the expense of measuring the length of the fibres which distribute the TTC signals, both objectives can be attained.

Further work is needed to see whether it is possible to do even more with the test pulses, such as the fine BC clock adjustment. It could be envisaged, for instance, to tune the test-pulse timing to simulate the timing of the particles coming from the interaction point, including their time of flight and the detector response time. However, this part is very much subdetector-dependent and cannot be addressed here.

Two different methods of using test pulses are being considered. The first method consists of sending a test pulse followed by a L1A signal after a known delay (this functionality is available in the CTP). The second method consists of sending a test pulse which will produce a L1A signal through the normal level-1 trigger electronics. This can be used, for instance, in the calorimeter.

Figure 19-6 and Table 19-1 show the different delays involved under three conditions — test pulse followed by a test trigger from the CTP, test pulse generating a trigger, and beam collision generating a trigger. The timing adjustment with a test pulse will be considered as efficient if the adjustment of the delay applied to the L1A signal is the same in all three conditions.

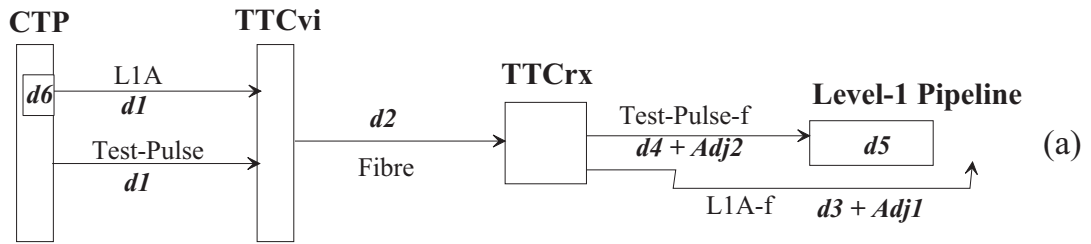
In the case [Figure 19-6(c)] of a beam-beam interaction producing a signal at the input of the pipeline at the time t_0 , the L1A will be generated at the time $t_0 + Latency$ and will reach the front-end at the time $t_0 + Latency + d1 + d2 + d3 + Adj1$ which must be equal to $t_0 + d5$. Hence one must have $Adj1 = d5 - Latency - d1 - d2 - d3$.

In the case [Figure 19-6(b)] of a test pulse which generates a L1A, one will have the following if one calls t_1 the time at which the test pulse is initiated at the TTCvi level:
 $t_1 + d2 + d4 + Adj2 + Latency + d1 + d2 + d3 + Adj1 = t_1 + d2 + d4 + Adj2 + d5$
 i.e. $Adj1 = d5 - Latency - d1 - d2 - d3$ which is identical to the value obtained with beam.

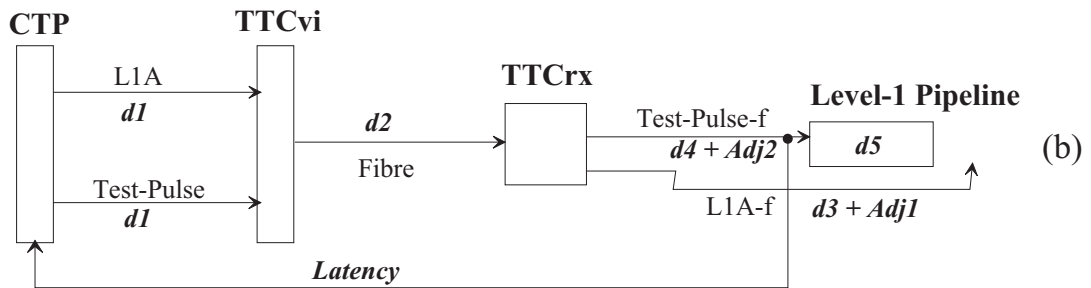
In the case where a pulse is sent by the CTP at the time t_2 , $d6$ microseconds before a L1A is generated, one needs to have:

Table 19-1 Delay elements

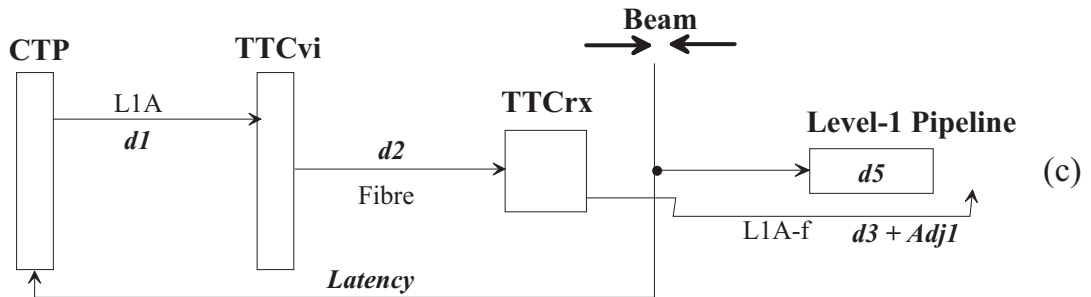
Delay	Meaning
$d1$	Cable delay from CTP to TTCvi
$d2$	Fibre length from TTC crate to TTCrx
$d3$	Latency on L1A (TTCvi + TTCrx)
$d4$	Latency on test-pulse (TTCvi + TTCrx)
$d5$	Pipeline length in time
$d6$	Delay between prepulse and L1A in the CTP
$Adj1$	Delay adjustment on L1A in TTCrx
$Adj2$	Delay adjustment on test-pulse in TTCrx
$Latency$	Level-1 latency up to the CTP output



Test Pulse followed by a L1A.
Time adjustment: L1A-f and Test-Pulse-f in the TTCrx



Test Pulse generating a L1A.
Time adjustment: L1A-f and Test-Pulse-f in the TTCrx



Beam generating a L1A.
Time adjustment: L1A-f in the TTCrx

Figure 19-6 Signal path and relevant timings (in italic).

$$t_2 + d1 + d2 + d4 + Adj2 + d5 = t_2 + d6 + d1 + d2 + d3 + Adj,$$

i.e.

$$Adj1 = d5 - d6 - d3 + d4 + Adj2.$$

Here, to have the same Adj1 value as with beam, one needs to have:

$$Adj2 = d6 - d4 - d1 - d2 - Latency$$

which can easily be achieved as all the different elements are known or easily measured. It only requires that the fibre length be measured at the installation time.

The procedure used to set up the timing is the following: the calculated $Adj2$ values are written in every TTCrx and a sequence of test-pulse-followed-by-L1A is started. A scan on all the $Adj1$ values is then done until the test-pulse signal is correctly seen in the readout data.

To check that the value used for the LVL1 latency is correct, all of the $Adj1$ values are then written in every TTCrx and the system is run in the mode described in Figure 19-6(b). If the timing set-up has to be changed, the LVL1 latency is not correct.

The absolute BCR adjustment cannot be treated here as it requires the beam. Nevertheless, the relative BCR adjustment between different subdetector parts and between subdetectors can be done as it just requires an arbitrary BCID = 0 to be defined in the CTP.

19.4 Timing set-up for test or calibration with test pulses

For each subdetector one needs to be able to test the front-end electronics system and/or to calibrate it. Some timing set-up of test pulses and L1A signals are also necessary in this case, but in this mode of running the CTP is generally not involved and each subdetector (or part of a subdetector) can work independently. The test-pulse, as well as the associated trigger signal, is issued at the TTCvi level of a TTC partition. The different delay elements involved are shown in Figure 19-7.

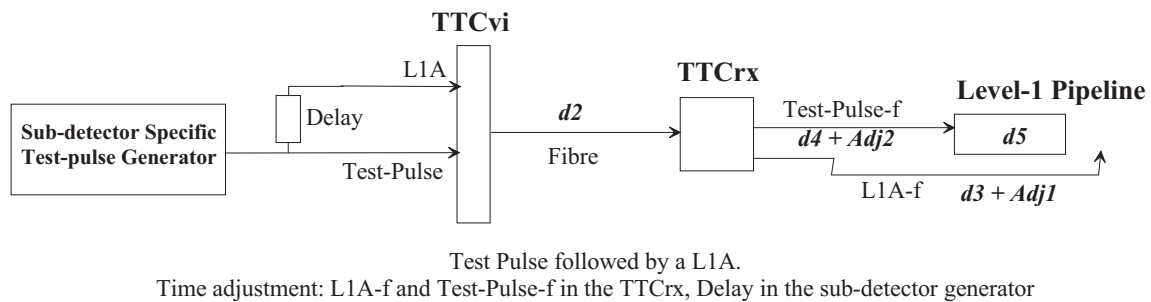


Figure 19-7 Signal path and relevant timings for sub-detector specific test-pulse/trigger generator.

The $Adj1$ and $Adj2$ values defined in Section 19.3 are generally not valid. Either they must be changed or some additional external delay elements must be introduced to make the local test-pulse / trigger timing sequence the same as the one obtained with the CTP.

19.5 References

- 19-1 *Trigger and DAQ Interfaces with Front-End Systems: Requirement Document (version 2.0)*, ATLAS note DAQ-NO-103, June 1998.
<http://www.cern.ch/Atlas/GROUPS/FRONTEND/FEreq980310.ps>