

21 Installation, access and maintenance

21.1 On-detector muon trigger electronics

Aspects related to the installation and maintenance of the on-detector muon-trigger electronics are to a large extent covered in the TDR for the muon system [21-1] and will be discussed in more detail in the forthcoming Technical Coordination TDR [21-2]. The on-detector muon-trigger subsystems require a significant amount of on-detector cabling, as well as cables between the detector and the USA15 counting room. Some of the electronics will be mounted on the chamber modules and some intra-module cabling will be carried out, prior to installation in the cavern. The remaining connections will be made at the time of installation.

21.2 General comments on electronics, cables and equipment

The electronics that are installed outside the cavern, either in the USA15 underground counting room or in surface buildings, will be mounted in standard racks. No special problems are foreseen with the installation or maintenance of this equipment. Nevertheless, the requirements analyses that have been performed have paid careful attention to issues of maintenance and repair.

The design of all of the trigger electronics, whether in the cavern or elsewhere, has to be such that faulty components (electronic modules, power supplies, backplanes, cooling units) can be replaced quickly. Other issues that have been addressed are the need for adequate supplies of spare parts, the availability at CERN of expert personnel during running periods and the need for test rigs at CERN.

Concerning the trigger-processor electronics, careful attention has to be given to the crate and rack layout, and to the routing of cables to, from, and within these electronics systems. A critical issue is the latency of the LVL1 trigger (see Chapter 18) for which propagation delays along electrical cables and optical fibres is a large contributor. In cooperation with the ATLAS Electronics Coordination and Technical Coordination groups, an optimal rack layout and cable routing has been devised that minimizes the overall latency. The LVL1 trigger team are working closely with the ATLAS Technical Coordination group on the routing of cables for electronics in the cavern and for connections between the cavern and USA15. The cable lengths that are used in the latency evaluations were calculated by the Technical Coordination team. The cable length calculations take into account the constraints that come from the need to open the detector for access without uncabbling. For the connections between the cavern and USA15, the shortest available path is taken through the shielding wall, whilst making sure that the radiation levels in USA15 will be safe for unlimited access by personnel.

Another aspect of cable routing that needs to be considered is related to the issues of maintenance and repair — cables should be routed in such a way that they do not prevent easy replacement of electronic modules. In practical terms, this means that it should be possible to replace any module in the system without massive recabbling of neighbouring modules in the system.

Apart from the custom electronics of the LVL1 trigger processors, there will be a significant amount of commercial electronics and computing equipment. This will include computers used to test, control, monitor and read out the trigger processors. No special problems of installation or maintenance are foreseen for this equipment which will be located in USA15 and also in surface buildings.

The issues discussed here, as well as the installation schedule for the cables and electronics, will be addressed in detail in the forthcoming Technical Coordination TDR [21-2].

21.3 References

- 21-1 *ATLAS muon spectrometer Technical Design Report*, CERN/LHCC/97-22, May 1997.
- 21-2 *ATLAS Technical Coordination Technical Design Report*, to be submitted to the LHCC.

22 Safety and environment

22.1 Introduction

A general description of the ATLAS safety aspects and the proposed risk-mitigation strategies is contained in the forthcoming Technical Coordination Technical Design Report [22-1]. This chapter deals only with those safety aspects particular to the LVL1 trigger system.

The LVL1 trigger system consists of electronics modules that are, with the exception of part of the muon trigger electronics, located in the USA15 underground counting room which is shielded against radiation.

The trigger system itself does not deal with large mechanical systems, high-voltage electrical equipment or flammable gasses. Part of the muon trigger system is mounted on the detector; the safety issues associated with the muon detector systems have already been documented [22-2].

The following sections discuss risks related to fire hazards, electricity and radiation, as well as associated considerations of access and cooling.

22.2 Fire safety

The LVL1 trigger system will contain a large number of electrical cables and optical fibres. Standard CERN rules [22-3] will be applied concerning the choice of cables. In particular, all cables will have a flame-resistant insulation that does not generate toxic fumes in case of fire.

The equipment located in the USA15 counting room will be mounted in standard CERN racks that include fire-detectors linked to the safety system in the experimental area. Damage to equipment in case of a localized fire (in cables, electronics modules or low-voltage power supplies) would be minimized by automatic fire-fighting equipment that would extinguish the fire using inert gasses. In such an eventuality, the automatic systems would also cut off the power supply to the associated equipment.

Issues relating to fire safety in the ATLAS cavern will be addressed in the forthcoming Technical Coordination Technical Design Report [22-1].

22.3 Electrical safety

Given the absence of high-voltage electrical equipment in the LVL1 trigger system, there are no particular electrical risks associated with personnel safety. Standard procedures and regulations will be followed concerning the use of equipment connected to the mains.

The LVL1 trigger systems, both in USA15 and in the cavern, require very high-current, low-voltage power supplies. As discussed above, these will be interlocked with the fire-protection systems. The Detector Control System, which will provide extensive monitoring of the low-

voltage systems (temperatures, voltages, currents) will detect problems and, if necessary, cut off the power supply in order to protect the equipment.

22.4 Radiation safety

A large part of the LVL1 trigger electronic system is located in the USA15 underground counting room that is well shielded against radiation. There are no radiation issues, either for personnel or for equipment, for this part of the system. The radiation levels will be sufficiently low to allow unlimited access to the USA15 area even when there is beam in the LHC machine.

Concerning the muon trigger electronics that is mounted in the cavern, and also the cables between the cavern and USA15, no radiation problems are expected from the point of view of personnel. This equipment is mounted on the outside of the detector, relatively well shielded from the interaction point, where there will be no significant activation. The overall CERN and ATLAS radiation protection policy will be followed.

Radiation issues do have to be taken into account in the design of the on-detector muon-trigger sub-systems as discussed in Chapters 9–14. In particular, all such electronics has to be tolerant to radiation up to the expected levels.

22.5 Access

As discussed in the Technical Design Report for the muon system [22-2] and in more detail in the forthcoming Technical Coordination TDR [22-1], appropriate passages and holes must be provided to allow access to the inner chambers for maintenance, repair, etc. In particular, these must allow access to the on-detector muon-trigger electronics for maintenance and repair operations.

22.6 Cooling

Issues of cooling will be addressed in the forthcoming Technical Coordination TDR [22-1], so only a very brief discussion is given here on matters relating to cooling of the LVL1 trigger electronics.

The equipment in the USA15 counting room will be mounted in racks with standard cooling systems. These will be fitted with temperature monitors and an interlock system that will cut off the electrical power supply in case of over heating.

The on-detector electronics associated with the RPC detectors will rely on natural air-cooling. As discussed in Chapter 12, active cooling is required for the on-detector electronics associated with the TGC detectors (higher density of electronics than in the RPC case). Temperature monitoring will prevent over-temperature situations causing damage to equipment; in case of a cooling failure (or any other over-temperature condition), the electrical power supply would be cut off.

22.7 References

- 22-1 *ATLAS Technical Coordination Technical Design Report*, to be submitted to the LHCC.
- 22-2 *ATLAS Muon Spectrometer Technical Design Report*, CERN/LHCC/97-22, May 1997.
- 22-3 CERN/TIS safety instruction, IS 23, *criteria and standard test methods for the selection of electrical cables, wires and insulated parts with respect to fire safety and radiation resistance.*

23 Project organization, management, schedule and costs

23.1 Participating institutes

The following list contains the institutes which are participating in the LVL1 trigger project, and the names of the physicists and senior engineers from each institute working on the project.

Birmingham

P. Bright-Thomas, A. Connors, J. Garvey, S. Hillier, R. Staley, P. Watkins, A. Watson.

CERN

I. Brawn, N. Ellis, P. Farthouat, P. Gallno, C. Havet, R. McLaren, G. Schuler, C. Schwick.

Haifa

N. Lupu, S. Robins, S. Tarem.

Heidelberg

C. Geweniger, P. Hanke, E-E. Kluge, J. Krause, K. Meier, U. Pfeiffer, A. Putzer, K. Schmitt, C. Schumacher, K. Tittel, M. Wunsch.

KEK

H. Iwasaki, T. Ohsaka, O. Sasaki, S. Tanaka, K. Yamauchi.

Kobe

K. Kawagoe, H. Kurashige, M. Nozaki, H. Takeda.

Kyoto

H. Sakamoto.

Lecce

P. Creti.

London QMW

E. Eisenhandler, M. Landon, J.M. Pentney.

Mainz

B. Bauss, K. Georgi, K. Jakobs, G. Quast, U. Schäfer.

Naples

A. Aloisio, F. Cavenini.

Rome I

A. Di Mattia, S. Falciano, L. Luminari, A. Nisati, E. Petrolo, S. Veneziano.

Rome II

R. Cardarelli, A. Di Ciaccio, R. Santonico.

RAL

J. Edwards, C.N.P. Gee, A.R. Gillman, R. Hatley, V.J. Perera, D.P.C. Sankey, T.P. Shah.

Shinshu

T. Takeshita.

Stockholm U

C. Bohm, M. Engström, S. Hellman, S. Silverstein.

Tel Aviv

S. Boettcher.

Tokyo ICEPP

Y. Hasegawa, K. Homma, M. Imori, T. Kawamoto, T. Kobayashi.

Tokyo MU

C. Fukunaga, R. Hamatsu.

Weizmann Institute of Science

E. Duchovni, E. Gross, D. Lellouch, L. Levinson, G. Mikenberg, K. Nagai.

23.2 Responsibilities and work organization

The LVL1 trigger system is divided into a number of subsystems between which interaction is limited. These are the calorimeter trigger, the muon trigger, and the central trigger (i.e. CTP and TTC systems). The muon trigger is further subdivided into the parts associated with the RPC detectors and the TGC detectors, and the part that forms the interface to the CTP. The institutes and funding agencies responsible for each of these parts are listed in the ATLAS Memorandum of Understanding [23-1]. A slightly more detailed list of responsibilities, also indicating the sharing of work within the calorimeter trigger and the muon trigger, is given in Table 23-1.

The work in each of the main areas (calorimeter trigger, muon trigger, central trigger) is organized largely independently. Issues of interfaces and where a common approach is needed are addressed in general LVL1 trigger working-group meetings and in *ad hoc* discussions between the groups concerned.

23.3 Management organization

The overall Trigger/DAQ project of ATLAS, covering the LVL1 and LVL2 triggers, the data acquisition and event filter, and the detector-control system, is organized in accordance with the normal ATLAS rules [23-2][23-3]. A Steering Group (see Table 23-2), with members representing different areas of the project, is the executive body responsible for managing the project as a whole. An Institutes Board, with one voting representative per institute, is responsible for deciding policy and for matters related to resources. Technical and scientific matters are discussed in working-group meetings for different areas of the project and in more specialized *ad hoc* working meetings. Responsibility for leading the project is currently shared between two coordinators, N. Ellis responsible for the trigger, and L. Mapelli responsible for the data acquisition and event filter. Steering Group meetings are chaired by one or other of the coordinators. The Institutes Board is presently organized by co-chair-people, M. Abolins and J.R. Hansen, who are *ex-officio* members of the Steering Group.

Table 23-1 Sharing of responsibilities for LVL1 trigger project

Item	Funding agencies	Institutes
Calorimeter trigger		
Front-end preprocessor	Germany (BMBF)	Heidelberg
Cluster processor (e/ γ , h/ τ)	UK	Birmingham, London QMW, RAL
Jet/energy-sum processor	Germany (BMBF), Sweden	Mainz, Stockholm
Processor readout system	UK	Birmingham, London QMW, RAL
Muon trigger		
RPC-based part	Italy	Naples, Lecce, Rome I, Rome II
TGC-based part	Japan, Israel	KEK, Kobe, Kyoto, Shinshu, Tokyo ICEPP, Tokyo MU; Haifa, Tel Aviv, Weizmann
Interface to CTP	CERN	CERN
Central trigger		
Central trigger processor	CERN	CERN
TTC system	CERN	CERN

Table 23-2 Present composition (June 1998) of the Trigger/DAQ Steering Group.

Activity	Members(s)
DAQ Coordinator	L. Mapelli
Trigger Coordinator	N. Ellis
LVL1 calorimeter trigger	E. Eisenhandler
LVL1 muon trigger	E. Petrolo
LVL2 trigger	S. Falciano, P. Le Du, F. Wickens
DAQ	R. Jones, G. Mornacchi
Event Filter	F. Etienne
Detector Control System	H. Burckhart
Trigger Performance	T. Hansl-Kozanecki
FE electronics	Ph. Farthouat

As discussed in the preceding section, the LVL1 trigger project is divided into a number of sub-projects that interact only weakly. These are the calorimeter trigger, the muon trigger and the central trigger (CTP and TTC systems). Both of the calorimeter and the muon trigger are explicitly represented on the Steering Group; the central trigger is represented by the Trigger Coordinator.

The organization of the LVL1 calorimeter trigger sub-project is as follows. Two- or three-day meetings are held every few months, with participation from all of the collaborating institutes, at which progress is reviewed and plans are discussed. These generally take place either in one of the collaborating institutes or at CERN. A management board, with one representative per

institute, addresses issues of resources within the sub-project and is also the decision-making body for the LVL1 calorimeter trigger sub-project. Decisions are subject to approval by the Steering Group, for very major decisions the Institutes Board, and ultimately the ATLAS Collaboration Board.

For the muon trigger a similar scheme to that described above for the calorimeter trigger has been adopted for the overall sub-project management. Meetings are held every few months at which progress is reviewed and plans are discussed. These usually take place at CERN prior to each ATLAS week (four meetings per year). Decisions are subject to approval by the Steering Group, for very major decisions the Institutes Board, and ultimately the ATLAS Collaboration Board.

Responsibility for the central trigger lies with a single institute (CERN). Progress is reviewed and plans are discussed in regular meetings. As for the other parts of the system, significant decisions are subject to approval by the Steering Group, for very major decisions the Institutes Board, and ultimately the ATLAS Collaboration Board.

Monitoring of the LVL1 project and its sub-projects takes place at a number of levels, firstly within each sub-project, then within the T/DAQ system, and finally ATLAS-wide. Monitoring is achieved through technical discussions in meetings that review plans and progress, by the work of the sub-project leaders and the overall Trigger Coordinator, and via formal reviews. Several levels of review are planned — internal reviews organized by the T/DAQ community and ATLAS reviews organized by the Technical Coordination group (e.g. Production Readiness Reviews). Regular progress checks will be made with the milestones defined in the detailed schedules, following the procedures defined by the ATLAS Technical Coordination group. Major milestones that can be used by the LHCC to monitor the progress of the project are proposed.

23.4 Schedule and milestones

In this section we list milestones for each of the major components of the level-1 trigger. Detailed schedules are given in their respective chapters:

- calorimeter trigger — Section 8.9;
- barrel muon trigger — Section 11.5;
- endcap muon trigger — Section 12.14.1;
- muon trigger CTP interface — Section 13.8;
- CTP — Section 15.7;
- TTC — Section 16.9.

23.4.1 Calorimeter trigger

Table 23-3 Milestones for the level-1 calorimeter trigger.

Milestone	Date
Calorimeter trigger system specifications completed	1998 Q4
Final Design Review for PPrASIC	2000 Q4
Final Design Review for PPrMCM	2000 Q4
Final Design Review for CPASIC	2001 Q2
Final Design Review for CPMCM	2001 Q2
Final Design Review for CP and JEP ROD module	2001 Q2
Final Design Review for PPM	2001 Q4
Final Design Review for JEM	2001 Q4
Final Design Review for CPM	2002 Q3
Preprocessor system tests completed	2003 Q4
Cluster Processor system tests completed	2004 Q2
Jet/Energy-sum Processor system tests completed	2004 Q2
Preprocessor system integrated with calorimeters	2004 Q3
Calorimeter trigger system commissioning completed for cosmic ray run	2004 Q4

23.4.2 Muon trigger

Table 23-4 Milestones for the level-1 muon trigger.

Milestone	Date
Muon endcap trigger readout protocol fixed	1999 Q4
CTP interface preliminary design review	2000 Q1
Muon barrel trigger coincidence matrix final design review	2000 Q1
Muon barrel trigger pad logic final design review	2000 Q3
Muon endcap trigger first full system test	2000 Q3
Muon barrel trigger readout driver final design review	2001 Q1
Muon barrel trigger sector logic final design review	2001 Q1
Muon barrel trigger optical link final design review	2001 Q1
Muon endcap trigger full system test before mass production	2001 Q3
CTP interface final design review and PRR	2002 Q2

23.4.3 CTP and TTC

Table 23-5 Milestones for the level-1 CTP and TTC.

Milestone	Date
CTP preliminary design review	1999 Q1
TTC crate preliminary design review	1999 Q4
TTCvi preliminary design review	1999 Q4
TTC crate final design review and PRR	2000 Q2
TTCrx preliminary design review	2000 Q2
TTCvi final design review and PRR	2000 Q3
TTCrx final design review	2000 Q4
CTP final design review and PRR	2001 Q1

23.5 Cost and resources

The ATLAS Collaboration has the necessary resources to build the level-1 trigger, as described in the Memorandum of Understanding [23-1]. The cost of the level-1 trigger is estimated to be as follows, in units of millions of ATLAS Swiss Francs (MASF), as defined in [23-4].

23.5.1 Calorimeter trigger

Table 23-6 Cost of the level-1 calorimeter trigger.

Item	Cost (MASF)
Preprocessor	2.417
Cluster Processor	3.334
Jet/Energy-sum Processor	1.230
Readout system (for CP and JEP)	0.287
Joint items (cables, computing, etc.)	0.394
Total	7.662

23.5.2 Muon trigger

Table 23-7 Cost of the level-1 muon trigger.

Item	Cost (MASF)
Barrel RPC trigger	2.605
Endcap TGC trigger	3.340
CTP interface	0.674
Total	6.619

23.5.3 CTP and TTC

Table 23-8 Cost of the level-1 CTP and TTC.

Item	Cost (MASF)
Central Trigger Processor	0.533
Timing, Trigger and Control system	1.308
Total	1.841

23.6 References

- 23-1 *Memorandum of understanding for collaboration in the construction of the ATLAS detector*, RRB-D98-44, April 1998.
- 23-2 *ATLAS Organization*, ATLAS note GEN-NO-09, 1994.
- 23-3 *ATLAS System Organization*, ATLAS note GEN-NO-15, 1996.
- 23-4 *ATLAS Cost Planning*, Version 7.0, January 1998.

A Appendix: Product breakdown structure

10.1 LVL1 Trigger

10.1.2.1 LVL1 Calorimeter Trigger Processor

- 10.1.2.1.1 Front-End Preprocessor
- 10.1.2.1.2 Cluster Processor
- 10.1.2.1.3 Jet/Energy-sum Processor
 - 10.1.2.1.3.1 Combined Items
 - 10.1.2.1.3.2 Jet Trigger Modules
 - 10.1.2.1.3.3 Energy-sum Trigger Modules
- 10.1.2.1.4 Readout System
- 10.1.2.1.5 Joint Items

10.1.2.2 LVL1 Muon Trigger Logic

- 10.1.2.2.1 LVL1 Muon Barrel Trigger Processor
 - 10.1.2.2.1.1 Low Pt Trigger
 - 10.1.2.2.1.1.1 Local Logic Board
 - 10.1.2.2.1.1.1.1 Coincidence Matrix Chip
 - 10.1.2.2.1.1.1.2 Pad Logic Board
 - 10.1.2.2.1.2 High Pt Trigger
 - 10.1.2.2.1.2.1 Local Logic Board
 - 10.1.2.2.1.2.1.1 Coincidence Matrix Chip
 - 10.1.2.2.1.2.1.2 Pad Logic Board
 - 10.1.2.2.1.3 Sector Logic
 - 10.1.2.2.1.4 Link from Sector Logic to Muon Interface to CTP
 - 10.1.2.2.1.5 Common Items
- 10.1.2.2.2 LVL1 Muon Endcap Trigger Processor
 - 10.1.2.2.2.1 Patch Panel
 - 10.1.2.2.2.1.1 Patch Panel Chip
 - 10.1.2.2.2.1.2 Patch Panel PCB for doublet wire
 - 10.1.2.2.2.1.3 Patch Panel PCB for doublet strip
 - 10.1.2.2.2.1.4 Patch Panel PCB for triplet wire
 - 10.1.2.2.2.1.5 Patch Panel PCB for triplet strip
 - 10.1.2.2.2.1.6 TTC receiver and distributor
 - 10.1.2.2.2.1.7 DCS port
 - 10.1.2.2.2.2 Slave Board
 - 10.1.2.2.2.2.1 Coincidence Matrix Chip
 - 10.1.2.2.2.2.2 Doublet Slave Board PCB for wire
 - 10.1.2.2.2.2.3 Doublet Slave Board PCB for strip
 - 10.1.2.2.2.2.4 Triplet Slave Board PCB for wire
 - 10.1.2.2.2.2.5 Triplet Slave Board PCB for strip
 - 10.1.2.2.2.3 High Pt Board
 - 10.1.2.2.2.3.1 Coincidence Matrix Chip
 - 10.1.2.2.2.3.2 High Pt Board PCB for wire
 - 10.1.2.2.2.3.3 High Pt Board PCB for strip
 - 10.1.2.2.2.3.4 High Pt crate
 - 10.1.2.2.2.4 Link from High Pt Board to Sector Logic
 - 10.1.2.2.2.5 Sector Logic
 - 10.1.2.2.2.5.1 Phase adjust
 - 10.1.2.2.2.5.2 R-Phi Coincidence Matrix
 - 10.1.2.2.2.5.3 Track Pre-selector

- 10.1.2.2.2.5.4 Track Selector
- 10.1.2.2.2.5.5 Track Encoder
- 10.1.2.2.2.6 Link from Sector Logic to Muon CTP Interface
- 10.1.2.2.2.7 Readout link from Slave Board to Star Switch
- 10.1.2.2.2.8 Star Switch
- 10.1.2.2.2.9 Readout link from Star Switch to ROD crate
- 10.1.2.2.2.10 ROD crate
 - 10.1.2.2.2.10.1 ROD
 - 10.1.2.2.2.10.2 Local DAQ Master
- 10.1.2.2.2.11 Common Items
- 10.1.2.2.3 LVL1 Muon Interface to Central Trigger Processor
 - 10.1.2.2.3.1 Octant Board [16]
 - 10.1.2.2.3.2 ROI - ROD Board
 - 10.1.2.2.3.3 Interface to CTP
 - 10.1.2.2.3.4 Crate [9U, VME]
 - 10.1.2.2.3.4.1 Readout Backplane
- 10.1.2.3 LVL1 Central Trigger Logic**
 - 10.1.2.3.1 Central Trigger Processor
 - 10.1.2.3.2 Deadtime Control
 - 10.1.2.3.3 Readout Driver
 - 10.1.2.3.4 LVL2 Interface
 - 10.1.2.3.5 Monitoring Tools
 - 10.1.2.3.6 Crate Processor
 - 10.1.2.3.7 Crate
 - 10.1.2.3.7.1 Readout Backplane
 - 10.1.2.3.7.2 ROD Busy Fan In/Out
- 10.1.2.4 Timing, Trigger and Control Distribution**
 - 10.1.2.4.1 TTC Crate
 - 10.1.2.4.2 TTCvi
 - 10.1.2.4.3 TTCrx

B Appendix: Definitions, acronyms, abbreviations

ADC

Analogue-to-digital converter.

AMUX

Analogue multiplexer.

ASD

Amplifier-shaper-discriminator circuit.

ASD-IC

Amplifier-shaper-discriminator integrated circuit.

ASIC

Application-specific integrated circuit. A custom-made integrated circuit.

ATLFAST

ATLAS software package for fast particle-level simulation.

ATRIG

ATLAS software package for trigger simulation.

Bakelite

RPC construction material: phenolic resin.

Barrel

The central-rapidity region of either the muon spectrometer, the electromagnetic calorimeter or the hadronic calorimeter.

Baud

Bits per second. Used for serial transmission; this rate is the total including all framing and protocol bits, as opposed to the net rate for transmitting actual data.

BC

Proton-proton bunch crossing in the LHC. The bunch spacing is 24.95 ns.

BCID

See Bunch-Crossing Identification.

BC-MUX; BC-multiplexing

Bunch-crossing multiplexing. Used in the Level-1 Calorimeter Trigger to double the number of trigger towers per serial link by using the fact that adjacent bunch-crossings cannot both carry valid trigger-tower data after BCID has been carried out.

BCR

See Bunch Counter Reset.

Bd

See Baud.

BER

Bit error rate.

BGA

Ball grid array.

Boundary scan (JTAG)

See JTAG.

BTL

Backplane transceiver logic. Devices intended for operation in the Futurebus+ signalling environment. They operate typically from +5 V power supplies, with signal lines terminated to +2.1 V. Receivers have a precise threshold (+1.55 V) for maximum noise immunity, and generated noise is minimized by incorporating slew-rate control.

Bunch Counter Reset (BCR)

Signal broadcast by the TTC system once per LHC orbit (88.924 s) to control the phase of local bunch counters.

Bunch-crossing identification (BCID)

The assignment of detector data to a specific bunch crossing.

Bunch_crossing_ID (ROD_BCID)

See ROD_BCID.

Calorimeter cell

The smallest unit of calorimeter information to be read out and digitized.

CAN

Control area network. A field bus for controlling and monitoring, used in the Detector Control System.

CCM

Clock Control Module of the Level-1 Calorimeter Trigger.

Central Trigger Processor (CTP)

The part of the Level-1 Trigger System which combines results from the Level-1 Calorimeter and Muon Triggers to make the global (yes/no) Level-1 Trigger decision for each bunch crossing.

CF

Cluster-finding.

Clock

The 40.08 MHz clock, linked to the LHC machine, used to synchronize the pipelined LVL1 processing system.

Cluster Processor

The part of the Level-1 Calorimeter Trigger that carries out the electron/photon and hadron/tau triggers.

CMM

Cluster Merger Module of the Level-1 Calorimeter Trigger.

CMOS

Complementary metal-oxide semiconductor. Switching logic with very low quiescent power dissipation. The logic levels are approximately equal to the supply voltage rails, covering a wide range down to +3 V. Compatibility with TTL is easily achievable.

CMS

Compact muon solenoid. The other 'general purpose' detector at the LHC.

CM

Coincidence matrix of the level-1 muon trigger.

CP

Cluster Processor of the Level-1 Calorimeter Trigger.

CPASIC

Cluster Processor ASIC of the Level-1 Calorimeter Trigger.

CPLD

Complex programmable logic device.

CPM

Cluster Processor Module of the Level-1 Calorimeter Trigger.

CPMCM

Cluster Processor multi-chip module of the Level-1 Calorimeter Trigger.

CPU

Central processing unit.

Counting room

See USA15.

CSC

Cathode strip chamber.

CTP

See Central Trigger Processor.

DAC

Digital-to-analogue converter.

DAQ

See Data Acquisition System.

Data Acquisition System (DAQ)

System responsible for the assembly and permanent storage of events accepted by all three levels of the trigger system (Level-1, Level-2, Event Filter) and data generated within the trigger systems.

DCS

See Detector Control System.

Derandomizer

The memory in which data corresponding to a Level-1 Accept are stored before being read out. The name is due to the fact that the data are available one event after the other whatever the time delays between successive Level-1 Accept signals was.

Detector Control System (DCS)

The system which monitors and controls physical parameters of the sub-systems of the experiment, such as gas pressure, flow-rate, high voltage settings, low-voltage power supplies, temperatures, leakage currents, etc.

DICE

ATLAS software simulation

DMA

Direct memory access: a mode of fast data transfer.

Doublet

Part of the muon spectrometer consisting of two layers of thin gap chambers.

DPMJET

Monte Carlo program used to generate simulated proton-proton interactions.

DSB

Doublet Slave Board of the muon endcap trigger.

DSL

Detector-specific logic. For each sector of the RPC and TGC systems provides an input to the muon-trigger/CTP interface.

ECL

Emitter-coupled logic. Refers to non-saturating, high-speed logic with a differential swing of ± 800 mV (-1.7 to -0.9 V), operating from a power-supply voltage of -5.2 V.

ECR

See Event Counter Reset.

EF

See Event Filter.

Electromagnetic isolation (e.m. isolation) region

A continuous region in the e.m. calorimeters, surrounding a potential electron/photon or hadron/tau cluster, whose summed transverse energy is used as a veto if it exceeds some (usually low) threshold. This is to help reject jet background.

Electron/photon cluster (e.m. cluster)

The areas in η - ϕ which are summed in the e.m. calorimeters in order to compare their transverse energy with electron/photon trigger thresholds. The elements used in the summing are e.m. Trigger Towers.

Electron/photon de-cluster/RoI region

The areas in η - ϕ which are summed in order to find local maxima in transverse energy, necessary for de-clustering electron/photon triggers and for electron/photon Regions-of-Interest. The elements used in the summing are e.m. Trigger Towers.

Electron/photon window

The areas in η - ϕ which are used for the electron/photon trigger algorithm, combining Electron/photon Clusters with isolation requirements in both the electromagnetic and hadronic calorimeters.

EMI

Electromagnetic interference.

Endcap

The high- η part of the muon spectrometer and calorimeter systems. The endcap covers the two ends of the cylindrical 'barrel' central region of ATLAS.

E.M.

Electromagnetic. (Can refer to either the calorimeters — e.m. vs. hadronic — or to the e.m. trigger, aimed at detecting electrons and photons.)

EPROM

Erasable programmable read-only memory.

Event

The data resulting from a particular bunch crossing. At high luminosity, this could contain data from several physics processes.

Event Counter Reset (ECR)

Signal broadcast by the TTC system to reset local event counters.

Event Filter (formerly level-3 trigger, or LVL3)

The third level of event selection, responsible for reducing the trigger rate and hence the data rate to a value acceptable for permanent storage, roughly 100 Mbyte/s. A processor system which receives events from the Event Builder, these events having been selected by L2_accept or L2_request signals. The Event Filter carries out further processing and analysis and, if accepted, sends the event to data storage for offline analysis.

Event_ID (EVID)

A number which identifies an event uniquely within a run.

FADC

Flash analogue-to-digital converter.

FCAL

Liquid-argon forward calorimeter.

FDR

Final design review.

FE

See Front End.

FE_BCID

A 12-bit number corresponding to the bunch number in the LHC machine, to identify the bunch crossing. It is generated locally in the RODs and reset by BCR. It is used to cross-check against ROD_BCID when identifying event fragments to be read out.

FE_L1ID

A number, of ≥ 4 bits, corresponding to the event number. It is generated locally in the RODs by counting Level-1 Accept signals. It is used to cross-check against ROD_L1ID when identifying event fragments to be read out.

FEM

Front-end Module. Used in the Level-1 Calorimeter Trigger demonstrator programme.

FIFO

First-in first-out. A type of buffer memory.

FIR

Finite-impulse response. A type of digital filter.

FLUKA

Monte Carlo program used to simulate e.m. and hadronic particle showers in the ATLAS detector. Used for radiation calculations.

Forward

The forward trigger refers to the inner (low-radius) part of the TGC trigger system.

FPGA

Field-programmable gate array.

Front End

Shorthand for Front-End Electronics.

Front-end electronics

The detector sub-systems which generate and send trigger data to the Level-1 Trigger System and event data to their RODs for transmission to the data acquisition system.

FWHM

Full-width at half-maximum. A measure of the width of a peak.

GE

Gigabit Ethernet.

GEANT

A general Monte Carlo simulation package for describing detector geometry and tracking particles through detector material. Used to simulate the response of the ATLAS detector.

GTL

Gunning transceiver logic. Operates typically from power supply voltages of +5 V or +3.3 V, with low-amplitude voltage swings of 0.8 V (+0.4 V to +1.2 V) for reduced power dissipation. Signal lines are terminated to +1.2 V, with a receiver comparator reference voltage of +0.8 V. Variants are available with driver slew-rate control to reduce e.m. interference and associated crosstalk.

H8

Test beam at CERN.

Hadronic isolation region

A continuous region in the hadronic calorimeters, behind a potential electron/photon cluster or surrounding a hadron/tau cluster, whose summed transverse energy is used as a veto if it exceeds some (usually low) threshold. This is to help reject jet background.

Hadron/tau cluster

The areas in η - ϕ which are summed in order to compare their transverse energy with hadron/tau trigger thresholds. The elements used in the summing are Trigger Towers.

Hadron/tau de-cluster/RoI region

The areas in η - ϕ which are summed in order to find local maxima in transverse energy, necessary for de-clustering hadron/tau triggers and hadron/tau Regions-of-Interest. The elements used in the summing are Trigger Towers summed over the combined depth of the electromagnetic and hadronic calorimeters.

Hadron/tau window

The areas in η - ϕ which are used for the hadron/tau trigger algorithm, combining hadron/tau Clusters with isolation requirements in both the electromagnetic and hadronic calorimeters.

HEC

Liquid-argon hadronic endcap calorimeter.

High- p_T board

Board of the muon trigger system which implements the high- p_T -muon trigger.

HV

High voltage

IC

Integrated circuit.

I²C

Inter-IC bus. Developed by Philips.

IEEE

Institute of Electrical and Electronics Engineers (USA).

IDR

Interim design review.

ISAJET

Monte Carlo program used to generate simulated proton-proton interactions for various physics processes, based on perturbative QCD plus phenomenological fragmentation models.

Isolation

See Electromagnetic (e.m.) Isolation and Hadronic Isolation.

JEM

Jet and Energy-sum Module of the Level-1 Calorimeter Trigger.

Jet de-cluster/RoI region

The areas in η - ϕ which are summed in order to find local maxima in transverse energy, necessary for de-clustering jet triggers and for jet Regions-of-Interest. The elements used in the summing are Jet Elements.

Jet element

The smallest elements in η - ϕ used to form transverse-energy sums for the jet trigger. The elements are summed over the combined depth of the electromagnetic and hadronic calorimeters. The size of these elements determines the step size for sliding the Jet Windows and Jet De-cluster/RoI Regions.

Jet/Energy-sum Processor

The part of the Level-1 Calorimeter Trigger that carries out jet, missing- E_T and scalar total- E_T triggers.

Jet window

The areas in η - ϕ which are summed in order to compare their transverse energy with jet trigger thresholds. The elements used in the summing are Jet Elements.

JMM

Jet Merger Module of the Level-1 Calorimeter Trigger.

JPM, JPMD

Jet Processor Module. Used in the Level-1 Calorimeter Trigger demonstrator programme.

JTAG (boundary scan)

A technique for loading data into or reading data out from a chip or a module using a single serial line that connects all relevant registers sequentially. The pin count is thus minimized. The standard for this is IEEE 1149.1; JTAG stands for Joint Technology Assessment Group.

L1A

See Level-1 Accept.

L1ID

See FE_L1ID.

L1MT

Level-1 muon trigger (system).

LAr

Liquid argon — refers to the ATLAS calorimeters, all of which except the Tile Calorimeter use liquid argon as a sampling medium.

LCANN

Local CAN node.

LDB

Local data-acquisition block of the muon endcap only trigger.

Level-1 Accept

A signal generated by CTP when an event has met the level-1 trigger criteria, i.e. is a level-1 trigger. It is distributed by the TTC system.

Level-1 calorimeter trigger

The part of the Level-1 Trigger System whose calculations are based on information from the ATLAS calorimeters. Trigger objects are e.m. showers, single hadrons (τ), jets, missing E_T , and total E_T .

Level-1 muon trigger

The part of the Level-1 Trigger System whose calculations are based on information from the ATLAS muon detectors. Trigger objects are high- p_T muons.

Level-1 trigger system (LVL1)

The first level of event selection, responsible for reducing the event rate from the bunch-crossing rate of 40 MHz to no more than 75 kHz averaged over short time periods (e.g. 10 ms), using a fast hardware processor. For accepted events, it issues Level-1 Accept to the front-end electronics and RoI_message to the Level-2 Trigger. The system consists of the Level-1 Calorimeter Trigger, the Level-1 Muon Trigger, and the Central Trigger Processor.

Level-2 trigger system (LVL2)

The second level of event selection, responsible for reducing the trigger rate from about 75 kHz (upgradable to 100 kHz) to a rate acceptable to the Event Filter, 1–5 kHz. It requests and receives RoI data from the ROBs and, after analysing it, sends an L2_accept or L2_reject signal for the event to the ROBs.

Level-3 trigger system

See Event Filter.

LHC

Large hadron collider.

LMB

Local control monitor board of the muon endcap trigger.

LS-Link

Local slave link. A cable link between slave boards in the muon endcap trigger logic via which data are read out.

LSB

Least-significant bit.

LSI

Large-scale integration. Refers to integrated circuits.

LUT

Lookup table.

LV

Low voltage.

LVDS

Low-voltage differential signalling. A high-speed (~500 Mbit/s) low-power, general-purpose interface standard. It features a low voltage swing of ± 400 mV (+1.0 V to +1.4 V) with power-supply voltages ranging from +5.0 V down to +2.7 V.

LVL1

See Level-1 Trigger System.

LVL1_A (LVL1_accept)

See Level-1 Accept.

LVL2

See Level-2 Trigger System.

LVL3

See Event Filter.

LVDS

Low-voltage differential signal.

LVPS

Low-voltage power supply.

L1A

See Level-1 Accept.

LynxOS

A real-time UNIX-like operating system from Lynx Real-Time Systems, Inc.

MATCH

A radiation tolerant GaAs transceiver chip used in the barrel muon trigger.

MCU

Micro controller unit.

MCM

Multi-chip module. Distinguished from hybrids by the use of bare integrated-circuit dies.

MDT

Monitored drift tube.

METRAL™

A family of connectors.

MGF

Morris Garages F-type. Four cylinder, sixteen valve, available in a variety of colours.

MIBAK

Backplane that connects modules of the muon-trigger/CTP interface.

MICTP

Module of the muon-trigger/CTP interface that drives data to the CTP.

MIOCT

Module of the muon-trigger/CTP interface that processes data for an area of the muon spectrometer equal to one octant in the azimuthal direction and half the detector in η .

MIROD

Module of the muon-trigger/CTP interface that supplies data to LVL2 (for RoI building) and the ROBs.

MSB

Most-significant bit.

MUCTPI

Muon-trigger-CTP interface.

NIM

A modular system of fast logic, used for trigger systems in particle-physics experiments in simpler times. Still in use, most commonly in test-beam triggering.

NRZ

Non-return to zero. A serial bit coding in which consecutive 1s do not need separators that go to zero.

Octant

A collection of TGCs, symmetric in ϕ , comprising one eighth of a muon TGC trigger plane.

OO

Object oriented. A methodology for writing software.

ORBIT

A signal transmitted by the LHC to the TTC at a fixed point in the LHC cycle. The ORBIT signal is the broadcast to the TTC partitions.

OS9

A real-time operating system, used mainly on single-board VME processors.

PBS

Product breakdown structure

PCB

Printed-circuit board.

PCI

Peripheral component interconnect. An industry-standard bus system used mainly in personal computers.

PDR

Preliminary design review.

PECL

Positive emitter-coupled logic. Refers to ECL circuitry operated with its power-supply voltage offset by +5.2 V, giving logic levels of +3.5 V and +4.3 V.

Pivot plane

Plane of chambers in the RPC or TGC system that defines the RoI position. Equivalent to 'reference plane'.

PLL

Phase-locked loop.

PMT

Photomultiplier tube.

PP

Preprocessor of the Level-1 Calorimeter Trigger.

PPG

Computer-controlled pulse generator.

- PPM**
Preprocessor Module of the Level-1 Calorimeter Trigger.
- PPS**
Prepulse. A signal that can be issued by the CTP a defined duration before an L1A. It is distributed to the front-end electronics by the TTC system and can be used to fire test pulses.
- Preprocessor**
The part of the Level-1 Calorimeter Trigger that digitizes the calorimeter signals, does bunch-crossing identification, and uses a lookup table to do pedestal subtraction, final E_T calibration, and apply a noise threshold.
- PRR**
Production readiness review.
- PPrASIC**
Preprocessor ASIC of the Level-1 Calorimeter Trigger.
- PPrMCM**
Preprocessor multi-chip module of the Level-1 Calorimeter Trigger.
- PS-Pack**
Patch-panel and slave-board package of the endcap muon trigger.
- PYTHIA**
Monte Carlo program used to generate simulated proton-proton interactions for various physics processes.
- QA**
See Quality Assurance.
- QAP**
Quality assurance plan. See Quality Assurance.
- Quality Assurance (QA)**
It's paperwork, but not as we know it. See PDR, IDR, FDR, URD, TP, TDR, PBS, WBS, PRR, and every other TLA you can think of.
- QCD**
Quantum chromodynamics.
- R&D**
Research and development.
- RAL**
Rutherford Appleton Laboratory.
- Readout Buffer (ROB)**
A standard module which receives data from the RODs via standard Readout Links, passes on request a subset of the data to the level-2 trigger, and buffers the data until a Level-2 Trigger decision has been reached whereupon, for accepted events, it transmits the data to the Event Filter.
- Readout Driver (ROD)**
The last element in the readout chain that is still considered part of the front-end electronics. This module collects one or more data streams from detector elements and merges them into a single stream which is fed via a standard Readout Link into a ROB.

Readout link

The ATLAS-standard data-transmission link between a ROD and a ROB.

Receiver station (formerly waveform-monitoring station)

Units into which analogue signals from the liquid-argon calorimeters are received and split. One output goes to the Level-1 Calorimeter Trigger front-end electronics, and the other is available for waveform monitoring by the calorimeter group.

Reference plane

Plane of chambers in the RPC or TGC system that defines the RoI position. Equivalent to 'pivot plane'.

Region-of-Interest (RoI)

A geographical region of the experiment, limited in η and ϕ , identified by the Level-1 Trigger System as containing candidates for Level-2 Trigger objects requiring further computation. Their data will be further analysed by the Level-2 Trigger System to decide if the event is to be processed further. In the case of B-physics triggers at low luminosity, some RoIs may be defined internally within the Level-2 Trigger.

RemASIC

Readout merger ASIC of the Level-1 Calorimeter Trigger.

Resistive Plate Chamber (RPC)

Muon detector used for triggering in the barrel region of ATLAS.

RMS (r.m.s.)

Root mean square.

ROB

See Readout Buffer.

ROC

Readout controller of the level-1 calorimeter trigger. This controls the transfers of data from the CPM to the ROD.

ROD

See Readout Driver.

ROD_BCID

A 12-bit number corresponding to the bunch number in the LHC machine, to identify the bunch crossing. It is provided by the TTC system to tag event fragments. This number will be reset with each LHC orbit (i.e. every 88.924 s).

ROD_BUSY

A signal to indicate that the ROD is busy, used to inhibit the level-1 trigger.

ROD_L1ID

A 24-bit number corresponding to the event number defined by counting Level-1 Accept trigger signals. It is provided by the TTC system to tag event fragments.

RoI

See Region-of-Interest.

RoI builder

A unit, inside the Level-1 Trigger System, that collects and formats level-1 RoI information for use by the Level-2 Trigger.

RoI_message

A signal sent from the Level-1 Trigger to the Level-2 Trigger which contains the coordinates of the Region-of-Interest.

ROM

Read-only memory.

RPC

See Resistive Plate Chamber.

RXM

Receiver module in the Receiver Stations.

SCT

Semi-conductor tracking detector.

Single-hadron/tau ...

See Hadron/tau ...

SL

Sector logic of the level-1 muon trigger.

SMM

Sum Merger Module of the Level-1 Calorimeter Trigger.

SRAM

Static random-access memory.

Star Switch

Network (e.g. Ethernet) device connecting a number of nodes in a star topology, allowing multiple simultaneous data transfers between different pairs of nodes at full speed.

SUSY

Super symmetry.

Tau/hadron ...

See Hadron/tau ...

TCM

Timing Control Module. Used in the Level-1 Calorimeter Trigger Demonstrator Programme.

TLA

Three-letter acronym.

TDR

Technical Design Report. What you are reading!

Thin Gap Chamber (TGC)

Muon detector system used for triggering in the endcap region of ATLAS.

Tile calorimeter (TileCal)

Hadronic barrel calorimeter, using scintillating tiles as active medium.

Timing, Trigger and Control (TTC)

The standard system which provides and distributes trigger signals (e.g. Level-1 Accept), timing signals (e.g. system clock timestamps), and control signals to the various sub-systems of the experiment.

- TOF** Time-of-flight.
- TP** Technical Proposal.
- Trigger** A decision made by a trigger system (LVL1 or LVL2) that a particular event is of potential interest and should be retained at least until the next stage of selection. At LVL1 and LVL2, this decision is based on a subset of data from the event.
- Trigger chamber** A generic term for RPCs and TGCs.
- Trigger menus** The set of trigger conditions in use at any particular time. They specify a list of items, each with threshold(s) and multiplicity, and the logic to be applied to them. The level-1 trigger menu is implemented in the CTP, and is a set of logical combinations of results from the Level-1 Calorimeter and Muon Triggers.
- Trigger tower** The smallest element of calorimeter information used in the Level-1 Calorimeter Trigger. It has dimensions of approximately 0.1×0.1 in η - ϕ and is summed over the full depth of either the electromagnetic or hadronic calorimeter concerned. Note that the number of Calorimeter Cells that have to be summed to produce a trigger tower ranges from 3 to 60.
- Triplet** Three layers of muon thin gap chambers.
- TRT** Transition-radiation tracking detector.
- TSB** Triplet slave board of the muon endcap only trigger.
- TTC** See Timing, Trigger and Control.
- TTCrx** TTC receiver chip.
- TTCvi** TTC VME interface module.
- TTL** Transistor-transistor logic. Refers to a family of saturating logic operated from a +5 V supply, with logic levels typically 0–0.3 V and 3.0–5 V for 0 and 1, respectively.
- TXM** Transmitter Module. Used in the Level-1 Calorimeter Trigger demonstrator programme.
- U** Unit of length used to measure rack height, equal to 1.75 inches.
- URD** User Requirements Document. Based (at least loosely) on software standard PSS-05 of the European Space Agency.

- URL**
Universal Resource Locator (address used by WWW).
- USA15**
The underground electronics cavern where the level-1 calorimeter trigger, with the exception of the muon barrel and endcap trigger logic, is located.
- VCXD**
Voltage-controlled oscillator.
- VDEC**
VLSI Design and Education Centre, University of Tokyo. A CAD centre for Japanese universities.
- VHDL**
VHSIC (Very high speed integrated circuit) hardware description language. A language for specifying the designs of electronic systems.
- VIC**
VME inter-crate connection. Used for both a standardized VME inter-crate bus, and for proprietary (Creative Electronic Systems SA) modules that implement it.
- VLSI**
Very Large Scale Integration. Refers to integrated circuits.
- VME; VMEbus**
Versa-Module Euro. A crate backplane bus system.
- Waveform monitor station**
See Receiver Station.
- WBS**
Work breakdown structure.
- Wire-group**
Group of wires that form a single readout unit in the TGC detector system.
- WWW**
World-Wide Web.
- ZEBRA**
A dynamic memory-management package for FORTRAN programs. Used in the ATLAS offline software.
- Zero suppression**
Compression of data by removal of values equal to zero.
- ZIF**
Zero insertion force (socket).

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