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“Radiation effects on electronic components and systems for LHC”

RADIATION EFFECTS ON ELECTRONIC COMPONENTS AND CIRCUITS

Second course: Radiation Effects on Electronics Circuits

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OUTLINE

1. **Cumulated irradiation effects on digital CMOS circuits**
    - Cumulated irradiation effects on CMOS transistors (reminder)
    - Cumulated irradiation effects on digital CMOS circuits;

2. **Cumulated irradiation effects on analogue circuits**

3. **Single Event Effects (SEE) on digital and analogue circuits**

4. **Summary**

1. Total dose effects on digital CMOS circuits

1.1. Total dose effects on CMOS transistors (overview)

reminder: Qox = density of oxide trapped charges (+); Qit = density of interface trapped charges (+ or -);
μ = carrier's *surface* mobility; Vtn and Vtp = threshold voltage for NMOS and PMOS;
Csc = capacitance of the depleted silicon under the oxide;
Sfi = slope of the drain current versus gate voltage characteristics in weak inversion mode.

a/ Total dose effects on basic CMOS parameters

- Qox ⇑ and Qit ⇑ => *Vtn ⇑ or ⇓, and Vtp ⇑*
- Qit ⇑ => μ ⇓
- Qit ⇑ => Csc ⇑

b/ Total dose effects on CMOS features:

- Vt ⇑ or μ ⇓ => Ron ⇑ $Ron = 1/[\mu.Cox(W/L).(Vgs-Vt)]$
- Vt ⇑ or μ ⇓ => Gm ⇓ $Gm = \mu.Cox(W/L).(Vgs-Vt)$
- Csc ⇑ => Sfi ⇓ $Sfi = (kT/q).Log(1+Cox/Csc)$

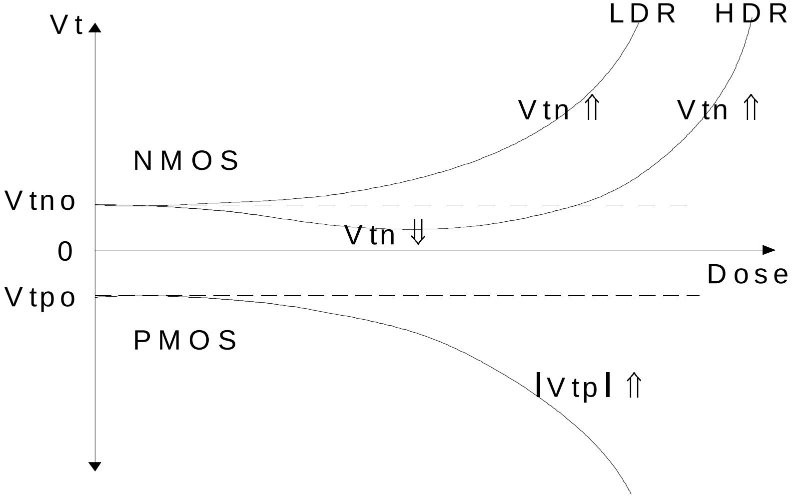
c/ Other total dose effects:

- Leakage current I_{intra} between drain and source of the same NMOS;
- Leakage current I_{inter} between adjacent NMOS.

d/ Displacement damages (NIEL): no effect on CMOS circuits.

Total dose effects on digital circuits, CMOS transistors - continued -

- **ΔVt depends on irradiation conditions:**



Low total dose + high dose rate:

Vtn ⇓ => Ron(n) ⇓ and Gm(n) ⇑
μ ⇓ => Ron(n) ⇑ and Gm(n) ⇓

The effect of μ dominates
=>Ron(n) ⇑ and Gm(n) ⇓

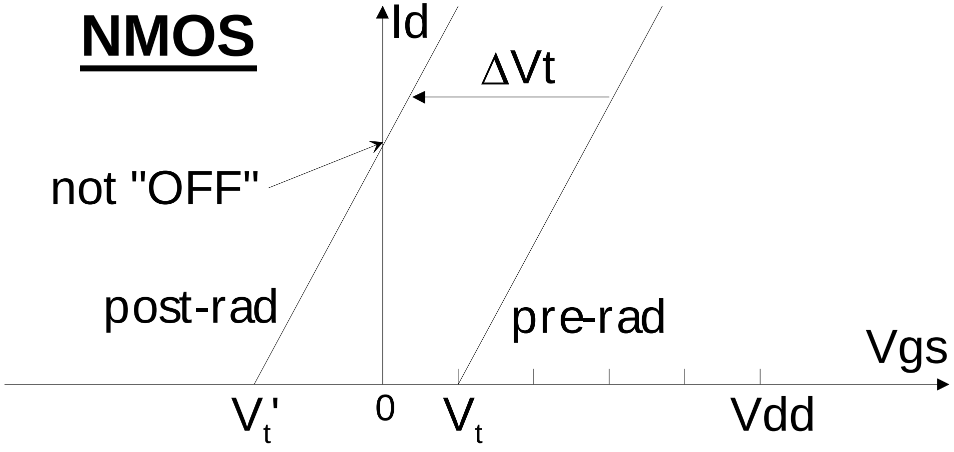
Vtp ⇑ => Ron(p) ⇑ and Gm(p) ⇓

High total dose, or low total dose + low dose rate:

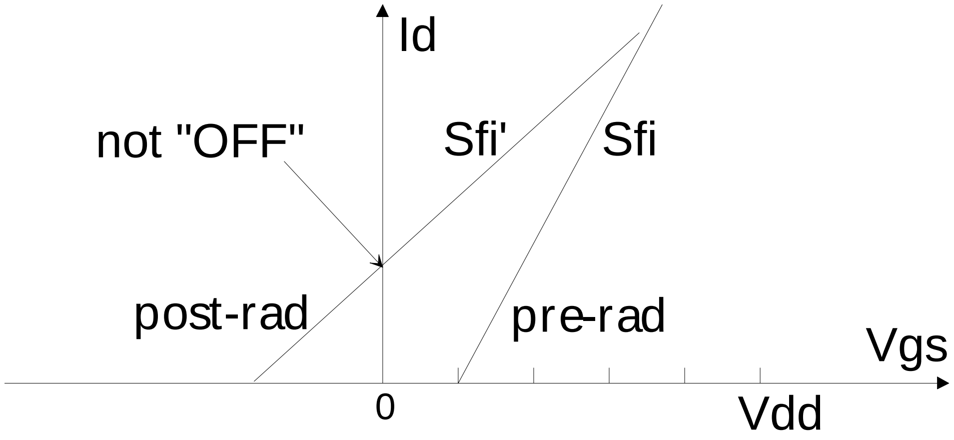
Vtn ⇑ =>Ron(n) ⇑ and Gm(n) ⇓
Vtp ⇑ =>Ron(p) ⇑ and Gm(p) ⇓

Total dose effects on digital circuits, CMOS transistors - continued -

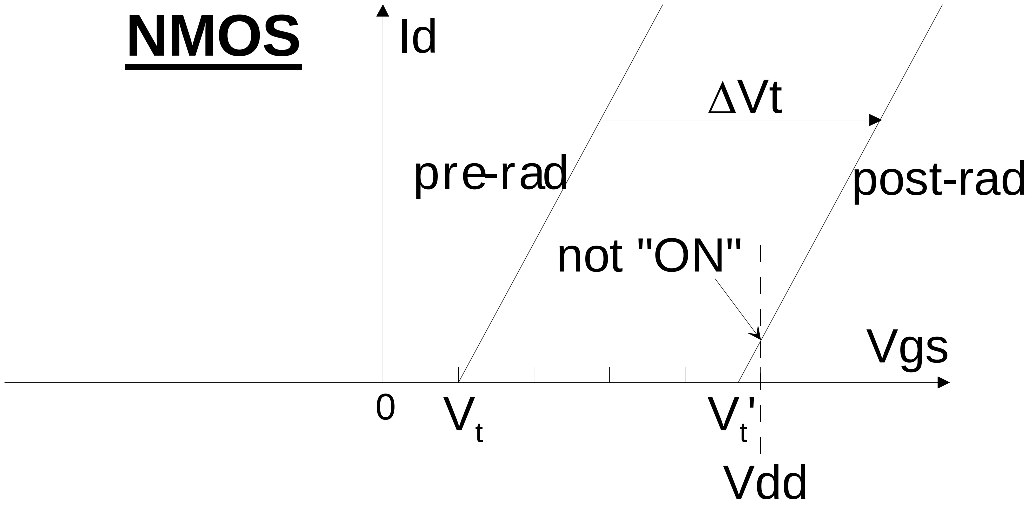
- **ΔVtn ⇓ can prevent NMOS “OFF” switching:**



- **Sfi ⇓ can prevent NMOS“OFF” switching:**

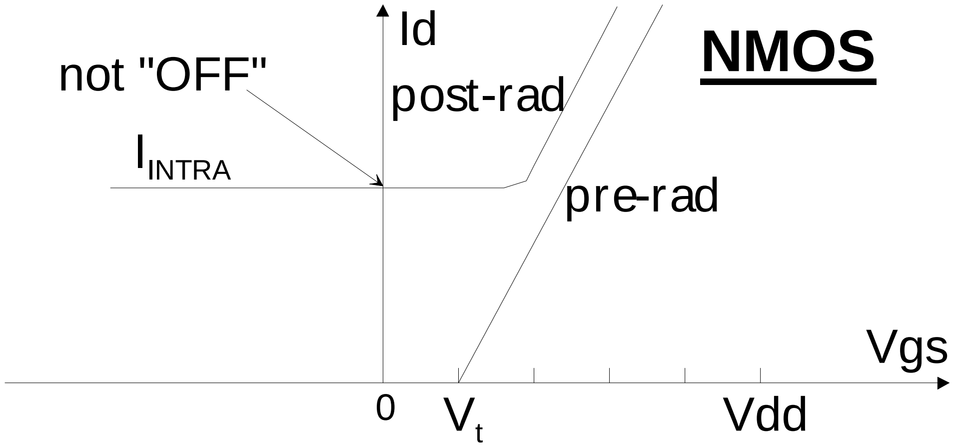


- **ΔVtn ⇑ can prevent NMOS “ON” switching:**



This risk increases when Vdd decreases.

- **I_{intra} <u>can prevent NMOS “OFF” switching:</u>**

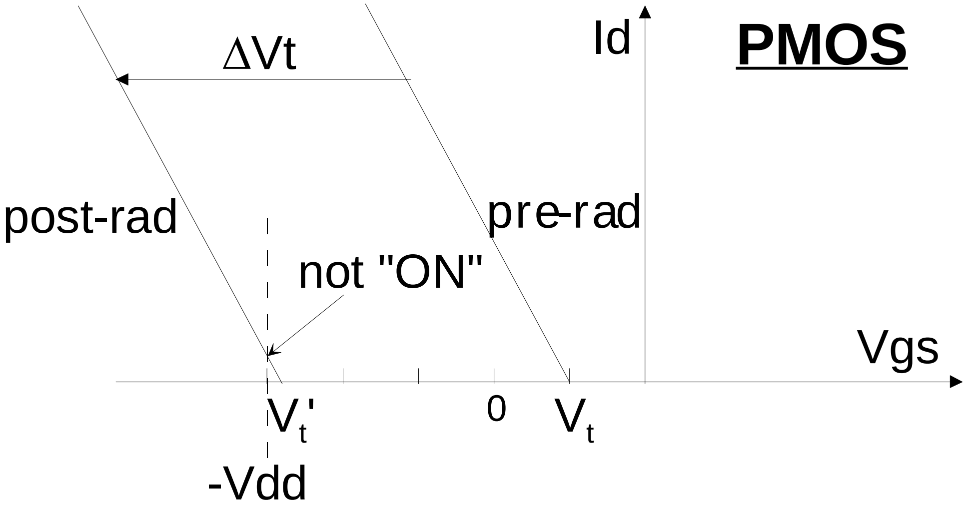


I_{intra} also induces a larger current consumption.

- **I_{inter} <u>disturbs or prevent the operation of the circuit:</u>**
  - Increase of the power consumption;
  - Abnormal operation, or no operation.

Total dose effects on digital circuits, CMOS transistors - continued -

- **ΔVtp ⇑ can prevent PMOS “ON” switching:**



This risk increases when Vdd decreases.

Radiation-hard technology:

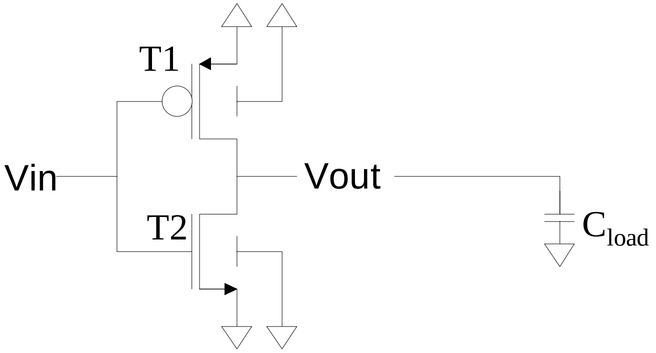
- ∆Gm, ∆Ron, ∆Sfi, and ∆Vt are small;
- ∆Sfi and ∆Vt are too small to prevent NMOS switching;
- No leakage current I_{intra} neither I_{inter} if the technology is submitted to a total dose complying with the specified radiation hardness.

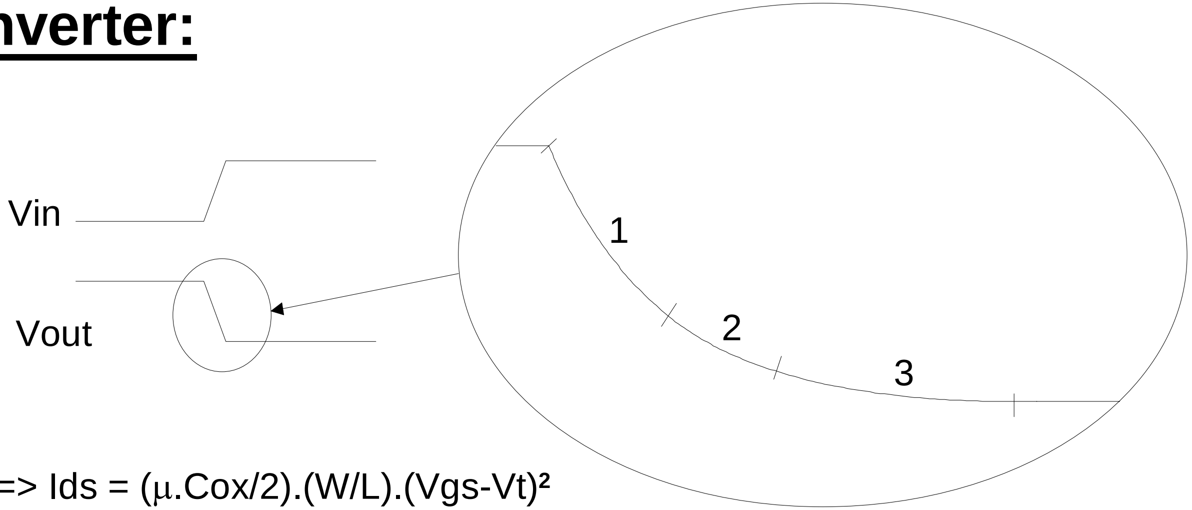
⇨ In the case of a radiation-hard technology used within the limits specified by the manufacturer, the total ionising dose induces only a widening of the worst case electrical parameters.

1.2. Total dose effects on digital circuits.

1.2.1. Static digital circuits

Example 1: inverter:





Region 1: $V_{ds} > (V_{gs}-V_t)$ => saturation => $I_{ds} = (\mu.C_{ox}/2).(W/L).(V_{gs}-V_t)^2$
=> $I_{ds} \sim \mu(\text{dose})$ and $V_t(\text{dose})$: **the rate of discharge decreases when the dose increases.**

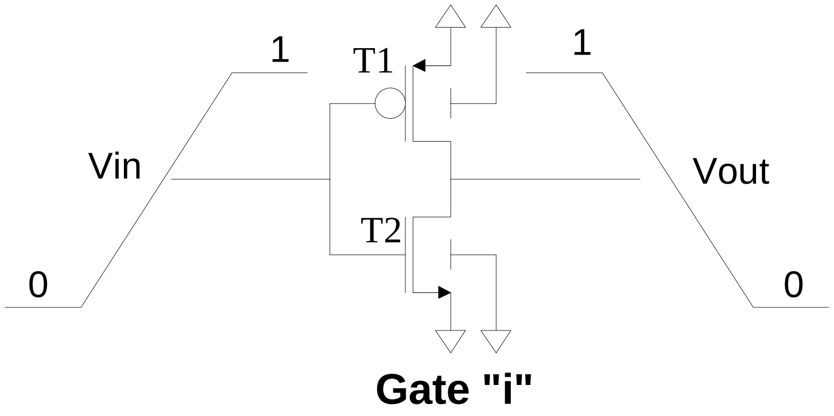
Region 2: $V_{ds} < (V_{gs}-V_t)$ => no saturation => $I_{ds} = (\mu.C_{ox}).(W/L).[(V_{gs}-V_t)V_{ds} - V_{ds}^2/2]$
=> $I_{ds} \sim \mu(\text{dose})$ and $V_t(\text{dose})$: **the rate of discharge decreases when the dose increases**.

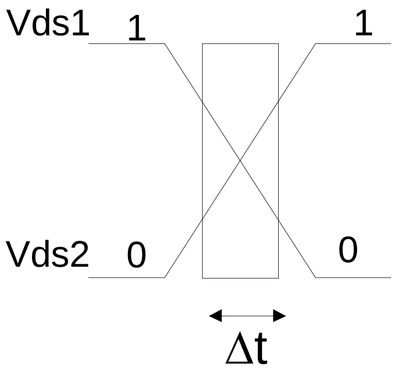
Region 3: $V_{ds}^2/2 \ll V_{ds}(V_{gs}-V_t)$ => $I_{ds} = (\mu.C_{ox}).(W/L).[(V_{gs}-V_t)V_{ds}]$
$\delta I_{ds}/\delta V_{ds} = (\mu.C_{ox}).(W/L).(V_{gs}-V_t) = 1/R_{on}$:
The chanel behaves as a resistor whose value increases with the dose.
=> $I_{ds} \sim 1/R_{on}(\text{dose})$: **the rate of discharge decreases when the dose increases**.

**=> The dose slows down the rising and falling edges.
This phenomenon is aggravated by the choice of a small Vdd.**

Total dose effects on static digital circuits: inverter - continued -

Dose => the switching speed decreases; the static and the dynamic consumption increase:





In the middle of switching, T1 and T2 are simultaneoulsy conducting => dynamic consumption.

Gate (i-1): The dose slows down the rising and falling edges Vin applied by gate (i-1) on gate (i).
Gate (i): the duration (Δt) of simultaneous conduction increases => the dynamic consumption increases
(Δt is also modified by ΔVt because the PMOS switching is delayed and the NMOS switching is modified, ...)
Also, the dose reduces the current Ids flowing in the MOS => the dynamic consumption decreases.

The results of these various mechanismes are generally an increase in the dynamic consumption and a decrease in the switching speed.

The increase in the dynamic consumption is generally masked by an increase in the static consumption induced by I_{INTER} et I_{INTRA} (except in the case of radiation hard technologies).

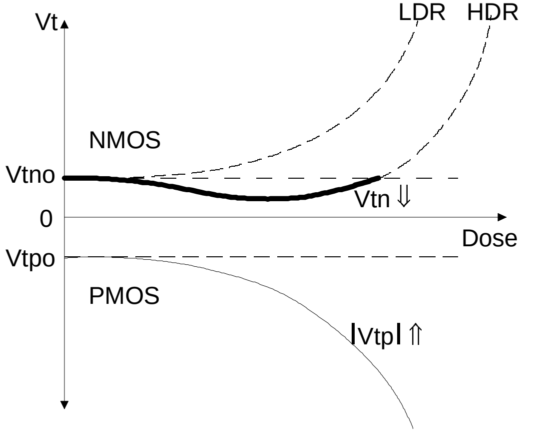
Total dose effects on static digital circuits: inverter - continued -

Summary of total dose effects on the inverter:

Low dose applied at high dose rate:

- Vtn ⇓ => faster 1 -> 0 switching
- μn ⇓ => slower 1 -> 0 switching
- Vtp ⇑ => slower 0 -> 1 switching
- μp ⇓ => slower 0 -> 1 switching
- C_{sc} ⇑ => Sfi ⇓
- Leakage currents I_{intra} and I_{inter}

The effect of μ dominates => slower 1 -> 0 switching



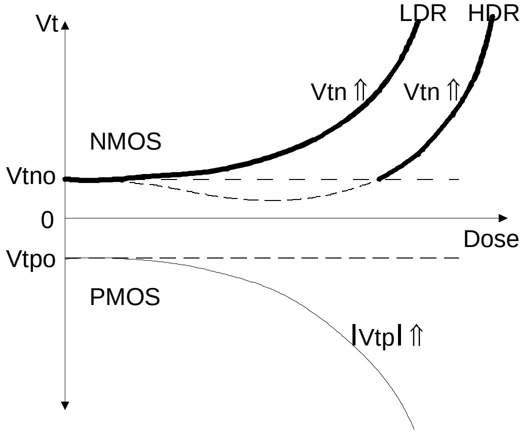
Consequences:

- Slower switching => *increased dynamic consumption*.
- I_{inter} ⇑ => *increased static consumption*.
- Vtp ⇑ can prevent PMOS “ON” switching => *risk of no switching*.
- Vtn ⇓ and Sfi ⇓ and I_{intra} ⇑ => NMOS are not fully “OFF” => V_{out} may be insufficient to define the state “1”. => *risk of no switching of the next gate*.

Total dose effects on static digital circuits: inverter - continued -

High dose, or low dose applied at low dose rate:

- Vtn ⇑ => slower 1 -> 0 switching
- μn ⇓ => slower 1 -> 0 switching
- Vtp ⇑ => slower 0 -> 1 switching
- μp ⇓ => slower 0 -> 1 switching
- C_{sc} ⇑ => Sfi ⇓
- Leakage currents I_{intra} and I_{inter}

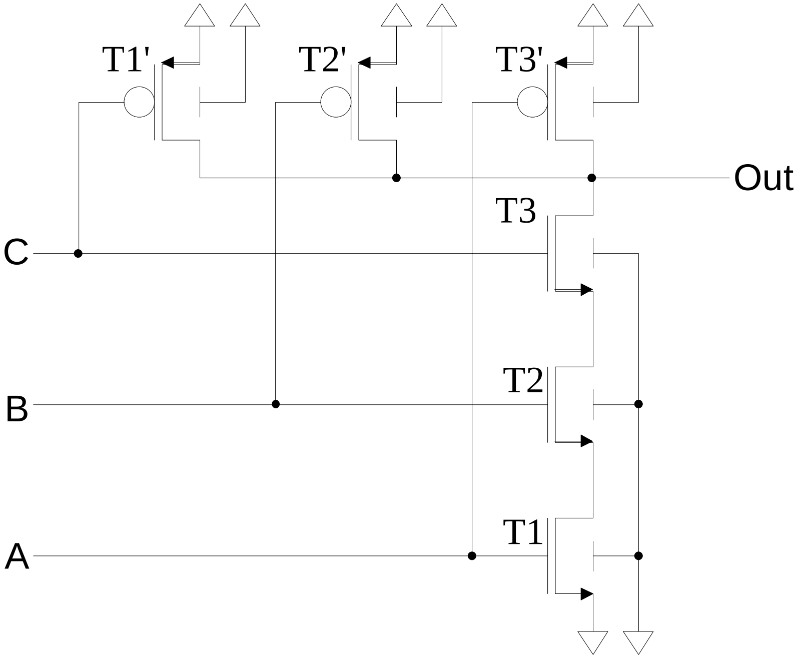


Consequences:

- Slower switching => *increased dynamic consumption*.
- I_{inter} ⇑ => *increased static consumption*.
- Vtp ⇑ can prevent PMOS “ON” switching => *risk of no switching*.
- Vtn ⇓ and Sfi ⇓ and I_{intra} ⇑ => NMOS are not fully “OFF” => V_{out} may be insufficient to define the state “1”. => *risk of no switching of the next gate*.

Total dose effects on static digital circuits - continued -

Example 2: NAND gate:



A	B	C	Out
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Total dose effects on static digital circuits, NAND gate - continued -

The switching speed decreases when the dose increases:

Fc ~ RC, with R = ΣRon ; C = Capacitance of the output node

Ron = $1/[(\mu C_{ox}).(W/L).(V_{gs}-V_t)]$ => Ron depends on μ, Vt and Vdd.

Dependence on μ(dose):

Dose ⇑ => μ ⇓ => Ron ⇑ => RC ⇑ => switching speed ⇓

Dependence on Vt(dose):

Vt = Vto + Vsb

Depending on precharge states, Vt (T2) and Vt(T3) >> Vto

=> slower switching of T2 and T3.

This mechanism is aggravated by Vt ⇑ (Vt shift induced by the dose).

⇨ Recommendation: if possible only 2 to 3 inputs maxi for NAND gates (replace NAND with n inputs by Σ NAND with 2 to 3 inputs)

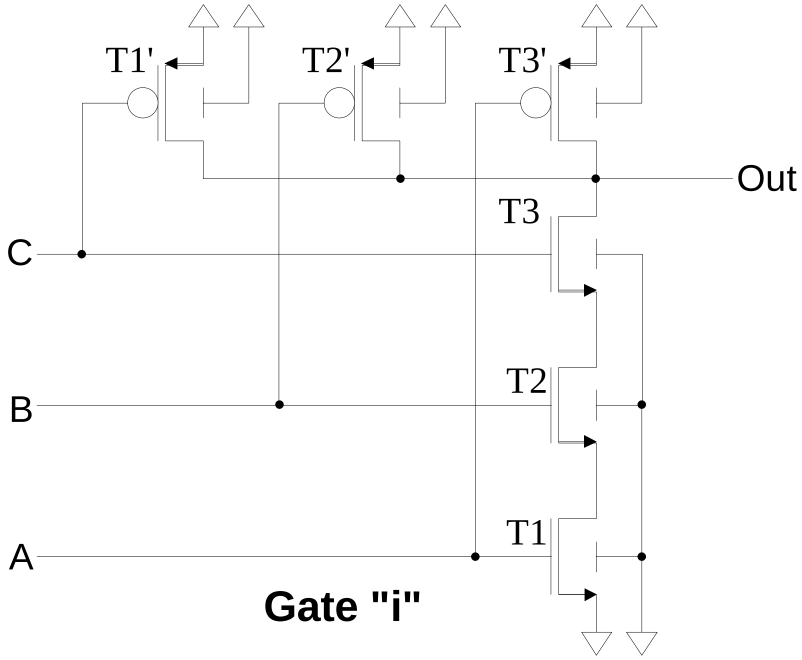
Role of Vdd:

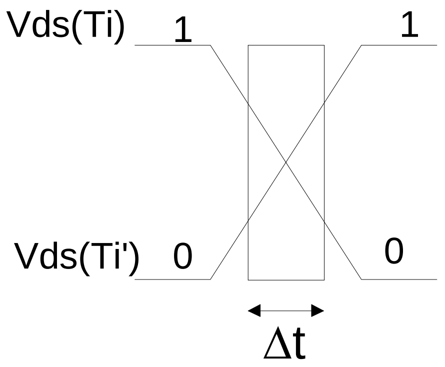
The choice of a small Vdd aggravates the slowing down induced by the dose.

⇨ Recommendation: choose Vdd as high as possible. (but: compromise between speed and power consumption)

Total dose effects on static digital circuits, NAND gate - continued -

Dose => the switching speed decreases; the static and the dynamic consumption increase:





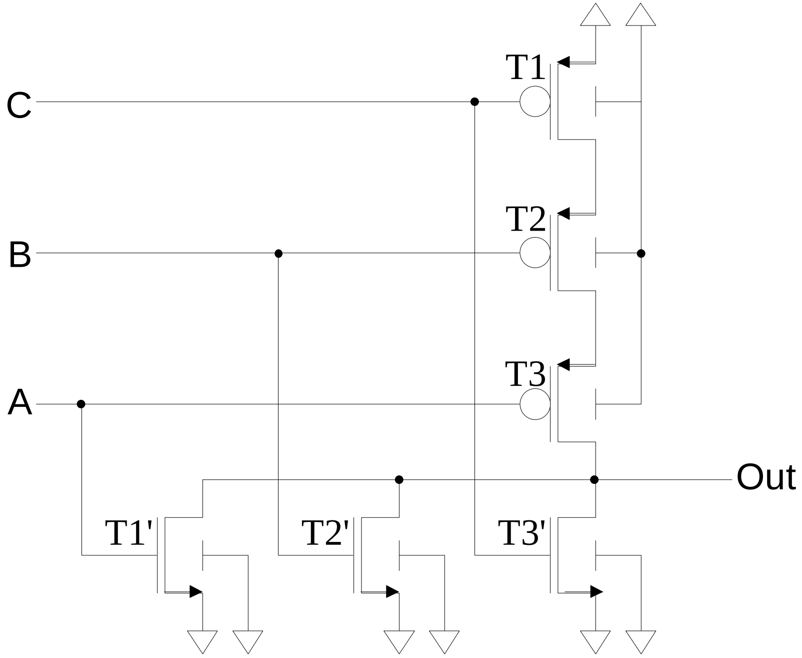
In the middle of switching, T and T' are simultaneoulsy conducting => dynamic consumption.

The various mechanisms discussed in the case of the inverter are also active in the case of the NAND gate. The results of these mechanisms are generally an increase in the dynamic consumption and a decrease in the switching speed.

The increase in the dynamic consumption is generally masked by an increase in the static consumption induced by I_{INTER} et I_{INTRA} (except in the case of radiation hard technologies).

Total dose effects on static digital circuits - continued -

Example 3: NOR gate:



A	B	C	Out
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

Total dose effects on static digital circuits, NOR gate - continued -

The switching of a NOR gate with n inputs implies the switching of n PMOS (instead of n NMOS in the case of a NAND gate)

$R_{on} = 1/[(\mu C_{ox}).(W/L).(V_{gs}-V_t)]$

μ (PMOS) << μ (NMOS) => Ron(PMOS) >> Ron(NMOS)

=> NOR switching speed << NAND switching speed

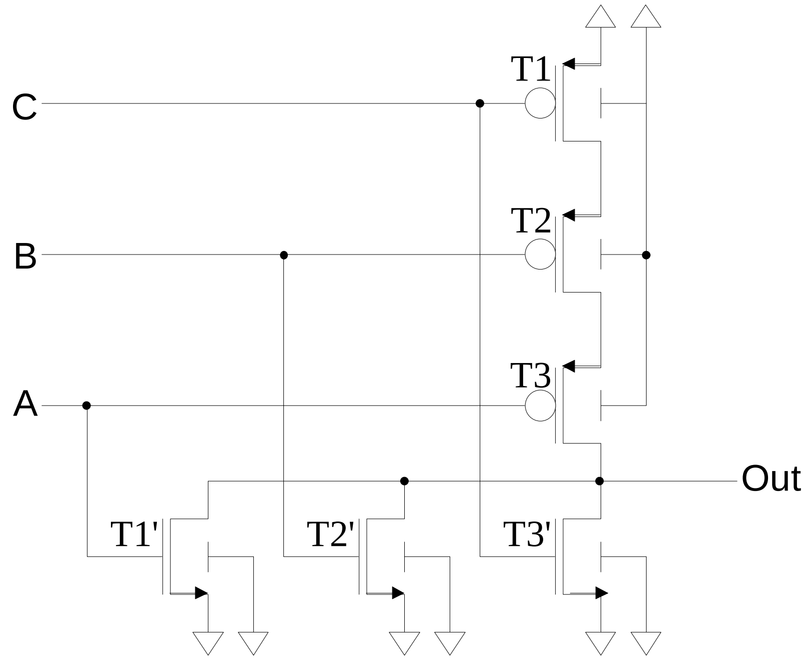
The dose slows down the switching speed and thus aggravates this effect.

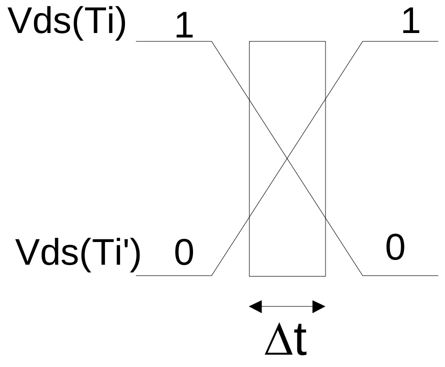
⇨ Recommendations:

1. replace NOR with n inputs by Σ NAND + inverter;
   (if possible 2 to 3 inputs maxi for the replacement NAND gates)
2. Choose Vdd as high as possible
   (compromise between speed and power consumption)

Total dose effects on static digital circuits, NOR gate - continued -

Dose => the switching speed decreases; the static and the dynamic consumption increase:





In the middle of switching, T and T' are simultaneoulsy conducting => dynamic consumption.

The various mechanisms discussed in the case of the inverter are also active in the case of the NOR gate. The results of these mechanisms are generally an increase in the dynamic consumption and a decrease in the switching speed.

The increase in the dynamic consumption is generally masked by an increase in the static consumption induced by I_{INTER} et I_{INTRA} (except in the case of radiation hard technologies).

Summary of the dose effects on static logic circuits:

- ΔVt => switching speed ⇓ then no commutation
- μ ⇓ => switching speed ⇓
- switching speed ⇓ => dynamic consumption ⇑
- Leakage currents => static consumption ⇑ then no commutation.

Remedies (compromise speed - consumption):

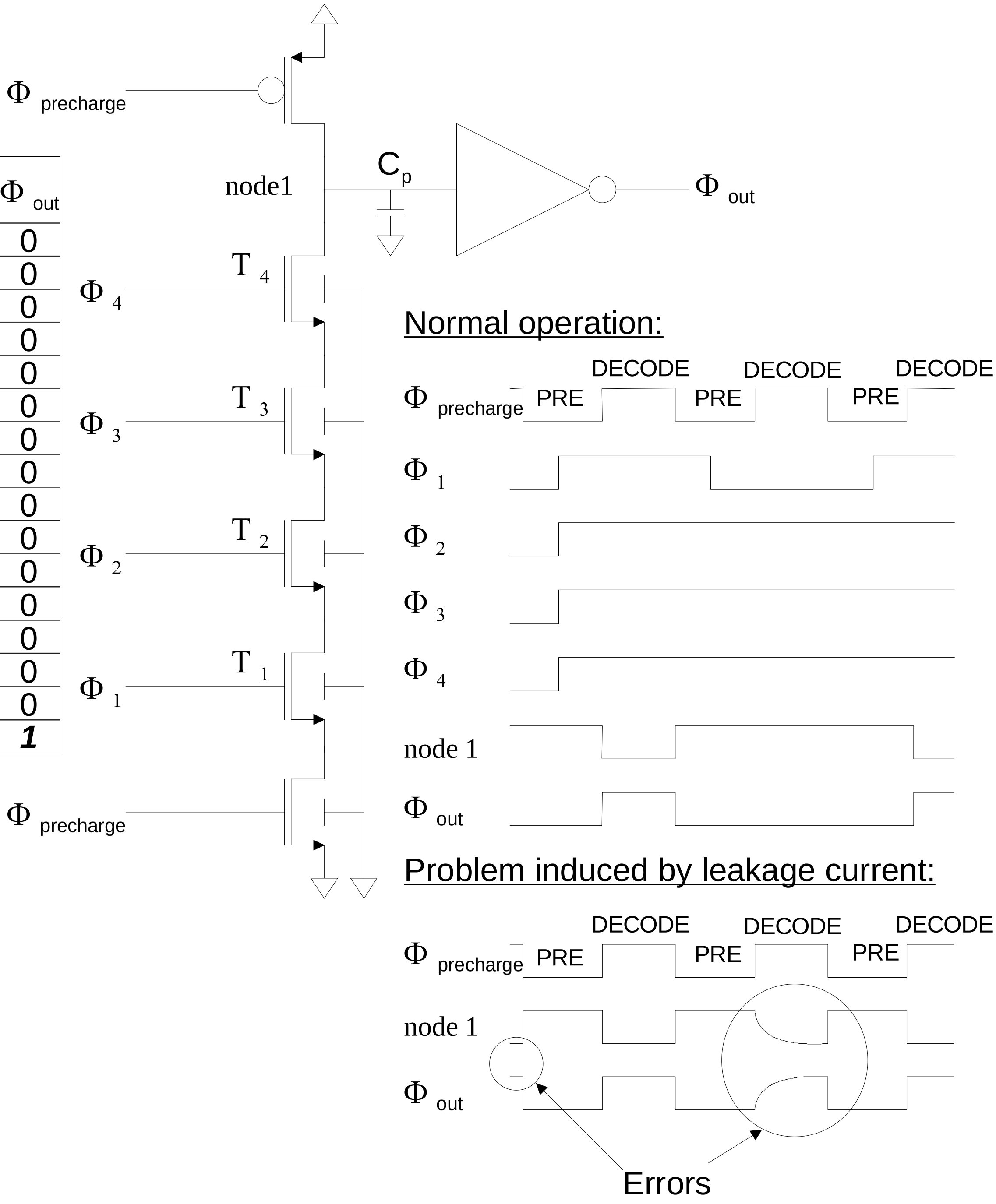
- Raise Vdd (=>ΔVt better tolerated, and Ron ⇓ and Gm ⇑ => speed ⇑)
- If possible 2 to 3 inputs maximum for NAND gates
- Replace NOR with n inputs by Σ NAND + inverter
- Raise W/L (=>Ron ⇓ and Gm ⇑ => speed ⇑)
  Remark: W/L ⇑ => C ⇑ => RC ⇑, but I increases faster than RC with W/L => the switching speed can be enhanced by W/L ⇑. The adjustment must be global in order that gate i-1 is not affected by problems of gate i (because gate i-1 see C ⇑ on gate i…).
- NMOS with a closed gate (but: C ⇑ => compromise with the speed)
- *If these remedies are not sufficient => Radiation-hard technology.*

Total dose effects on digital circuits - continued -

1.2.2. Total dose effects on dynamic logic circuits.

Example 1: dynamic NAND gate (element of PLA).

Φ_1	Φ_2	Φ_3	Φ_4	Φ_{out}
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	***1***	***1***	***1***	***1***



Total dose effect on dynamic NAND gate:

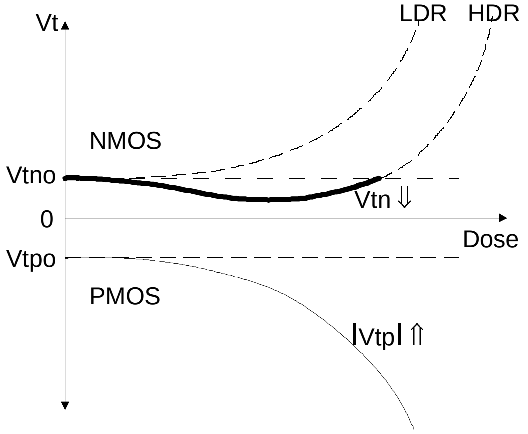
Low dose applied at high dose rate:

- Vtn ⇓ => faster 0 -> 1 switching
- μn ⇓ => slower 0 -> 1 switching

The effect of μ dominates
=> slower 1 -> 0 switching

- Vtp ⇑ => slower precharge
- μp ⇓ => slower precharge
- C_{sc} ⇑ => Sfi ⇓

  Leakage currents I_{intra} and I_{inter}



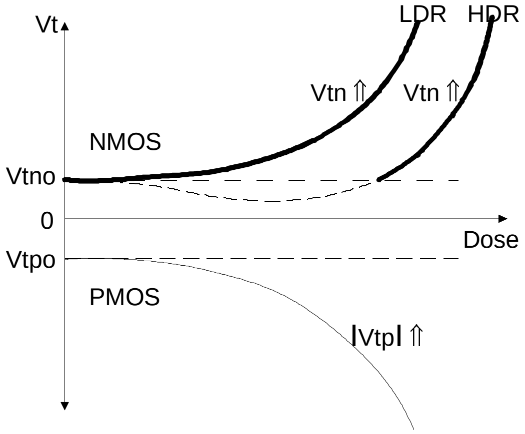
Other consequences:

- Slower switching => *increased dynamic consumption*.
- I_{intra} and I_{inter} => increased static consumption.
- Vtn ⇓, Sfi ⇓, I_{intra} ⇑ => NMOS not fully “OFF” => discharge of the precharge => low frequency operation not longer possible, or no operation.
- Vtp ⇑ can prevent PMOS “ON” switching => precharge can’t be done.

Total dose effects on dynamic digital circuits, NAND gate - continued -

High dose applied at low dose rate:

- Vtn ⇓ => slower 0 -> 1 switching
- μn ⇓ => slower 0 -> 1 switching
- Vtp ⇑ => slower precharge
- μp ⇓ => slower precharge
- C_{sc} ⇑ => Sfi ⇓
- Leakage currents I_{intra} and I_{inter}



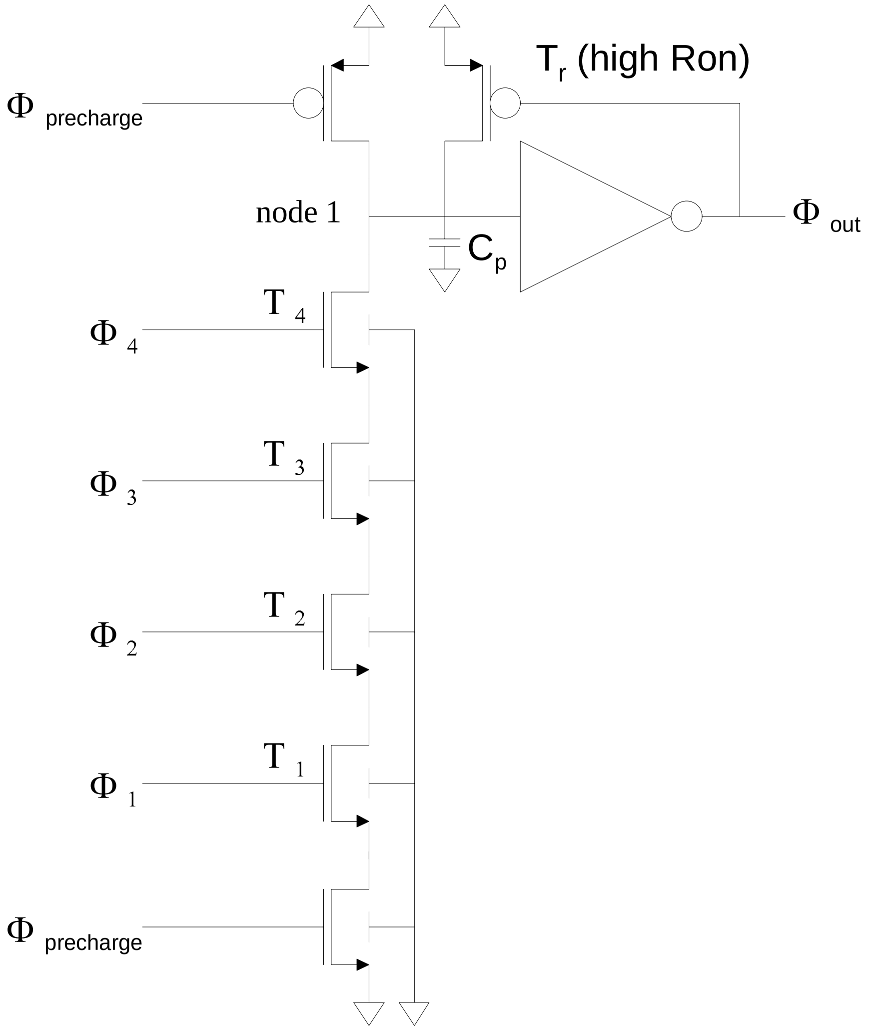
Other consequences:

- Slower switching => *increased dynamic consumption*.
- I_{intra} and I_{inter}=> increased static consumption.
- Vtn ⇓, Sfi ⇓, I_{intra} ⇑ => NMOS not fully "OFF" => discharge of the precharge => low frequency operation not longer possible, or no operation.
- Vtp ⇑ can prevent PMOS "ON" switching => precharge can't be done.

Total dose effects on dynamic digital circuits, NAND gate - continued -

How to maintain a precharge state?

⇨ quasistatic NAND gate:



- The precharge state is maintained by Tr.
- Ron (Tr) >> Ron (Ti) => switching OK.
- Not a solution if leakage current is too high.

Total dose effects on dynamic digital circuits, NAND gate - continued -

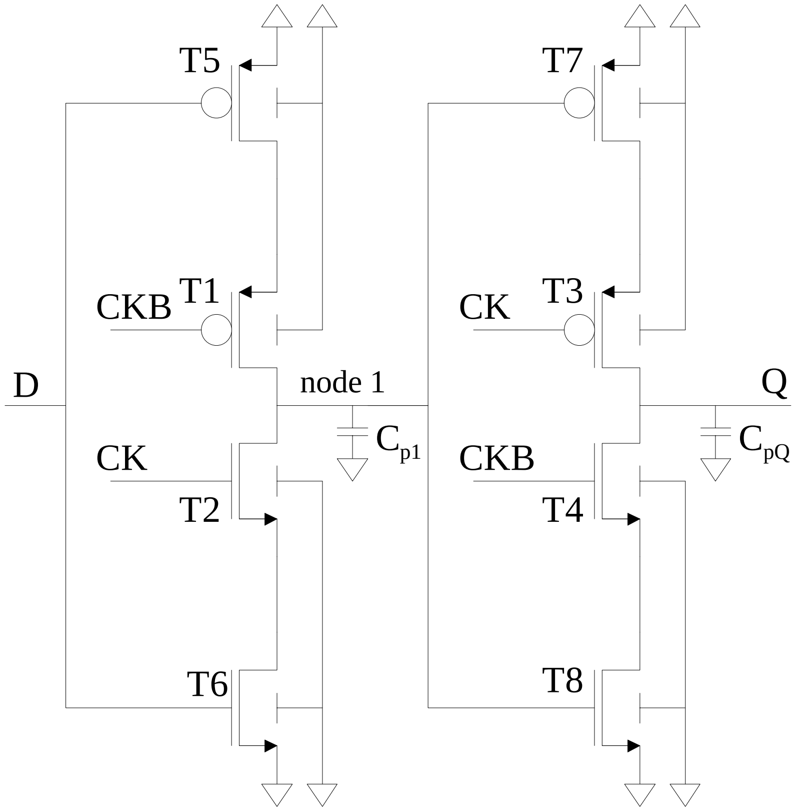
Radiation-hard Technology.

- ΔSfi and ΔVt are too small to prevent MOS switching;
- μn ⇓ and μp ⇓ can slow down the maximum operation frequency;
- No leakage current I_{intra} neither I_{inter} if the technology is submitted to a total dose complying with the specified radiation hardness => precharge states are not affected by the total dose => no problem of minimum operation frequency.

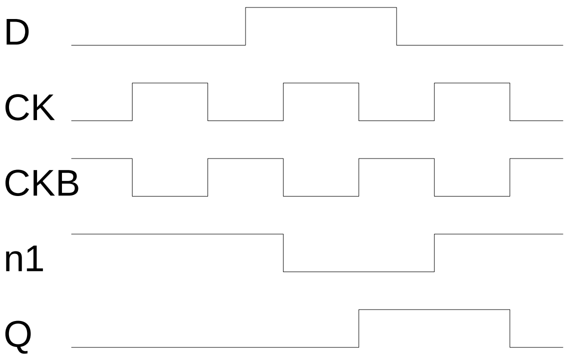
⇨ In the case of a radiation-hard technology used within the limits specified by the manufacturer, the total ionising dose induces only a slow down of the maximum operation frequency.

Total dose effects on dynamic digital circuits - continued -

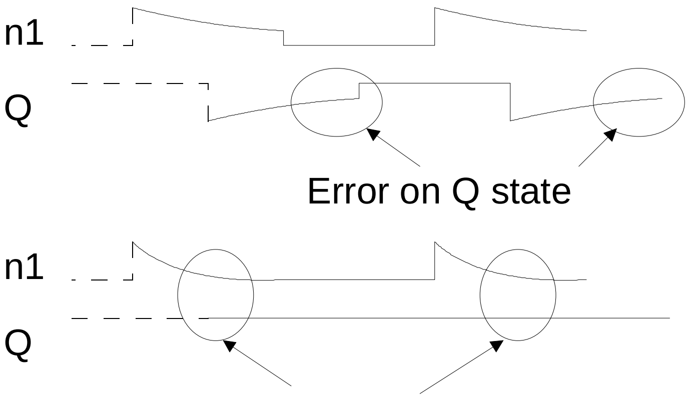
Example 2: dynamic D flip-flop.



Normal operation



Problem induced by leakage current



Error on Q state

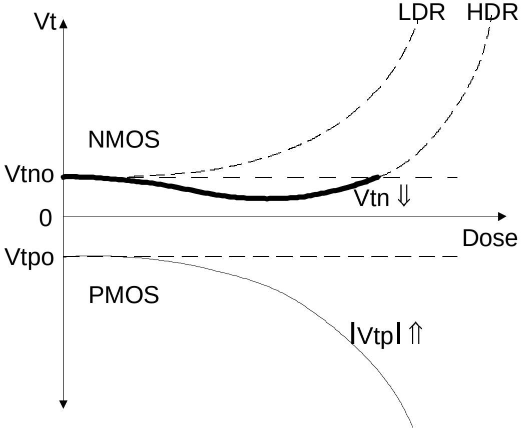
n1 state n1 = 0 (error)
=> Q doesn't switch

Total dose effect on dynamic D flip-flop:

Low dose applied at high dose rate:

- Vtn ⇓ => faster 1 -> 0 switching
- μn ⇓ => slower 1 -> 0 switching
- Vtp ⇑ => slower 0 -> 1 switching
- μp ⇓ => slower 0 -> 1 switching
- C_{sc} ⇑ => Sfi ⇓
- Leakage currents I_{intra} and I_{inter}

The effect of μ dominates
=> slower 1 -> 0 switching



Other consequences:

- Slower switching => *increased dynamic consumption*.
- I_{intra} and I_{inter}=> increased static consumption.
- Vtn ⇓, Sfi ⇓, I_{intra} ⇑ => NMOS not fully “OFF”

⇨ discharge of nodes n1 and Q ; no switching of Q

⇨ low frequency operation no longer possible, or no operation.

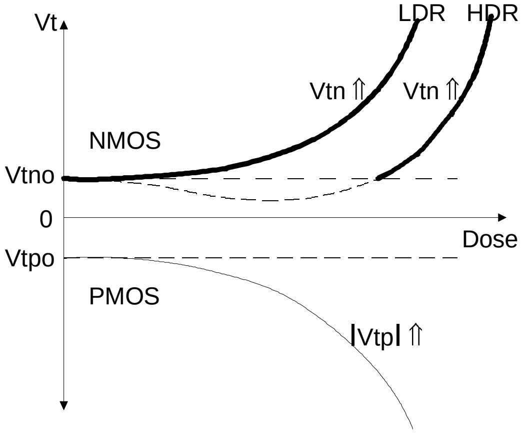
- Vtp ⇑ can prevent PMOS “ON” switching

⇨ 0 -> 1 switching is no longer possible.

Total dose effects on dynamic digital circuits, D flip-flop - continued -

High dose applied at low dose rate:

- Vtn ⇑ => slower 1 -> 0 switching
- μn ⇓ => slower 1 -> 0 switching
- Vtp ⇑ => slower 0 -> 1 switching
- μp ⇓ => slower 0 -> 1 switching
- C_{sc} ⇑ => Sfi ⇓
- Leakage current I_{intra} and I_{inter}



Other consequences:

- Slower switching => *increased dynamic consumption*.
- I_{intra} and I_{inter}=> increased static consumption.
- Vtn ⇑ can prevent NMOS “ON” => 1 -> 0 switching not possible
- Vtp ⇑ can prevent PMOS “ON” => 0 -> 1 switching not possible.
- I_{intra} => discharge of nodes n1 and Q ; no switching of Q
  ⇨ low frequency operation no longer possible, or no operation.

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Summary of total dose effects on digital circuits

- **Total dose effects:**
  - Switching speed ⇓
  - Dynamic consumption ⇑
  - Static consumption ⇑
  - No operation induced by no switching
  - No operation induced by loss of precharge (dynamic logic)

- **Remedies:**
  - Use the higher authorized Vdd
  - Prefer static logic to dynamic logic
  - Design tricks: limit the number of inputs on gates; replace NOR gates by NAND gates + inverters, oversize W/L, draw NMOS with closed gate and guard ring, …
  - (…)

If these remedies are not sufficient, use radiation-hard technologies.

2. Cumulated radiation effects on analogue circuits

2.1. CMOS amplifiers

a/ DC biasing:

- I and V biases are controlled by μ(dose), Vt(dose) and Vg(Vdd).
  $I = (\mu Cox/2).(W/L).(Vg-Vt)^2$
- Before irradiation: specifications are satisfied; circuits are robust with respect to the specified dispersion of electrical parameters.
- After irradiation: DC point is shifted (I decreased, V modified)
  - ⇨ possible violation of the specifications;
  - ⇨ loss of robustness with respect to the specified dispersion of electrical parameters.

Possible corrections:

- Raise Vdd to restore the initial current bias;
- Raise I_{bias} if tuneable from outside, in order to correct V
  - ⇨ *Limited corrections ; adjustment of Vdd => consumption ⇑.*

Cumulated radiation effects on analogue circuits, CMOS amplifiers – continued.

b/ Operation with small AC signals:

G.BW product ~ gm/C_{out}

- $gm = \mu.Cox.(W/L)(Vg-Vt) = 2[(\mu Cox/2).(W/L).I_{bias}]^{1/2}$
- dose ⇑ => $\underline{\mu \Downarrow}$ and Vtn ⇓ and Vtp ⇑ => gm ⇓ => G.BW ⇓

Possible corrections:

- Raise Vdd to increase gm;
- Raise I_{bias} if tuneable from outside, in order to restore gm
  - ⇨ *Make sure the circuit stays within the permitted DC conditions.*
  - ⇨ *Limited corrections ; adjustment of Vdd => consumption ⇑.*
- Add to the OA an architecture that stabilises gm [ref. 8]

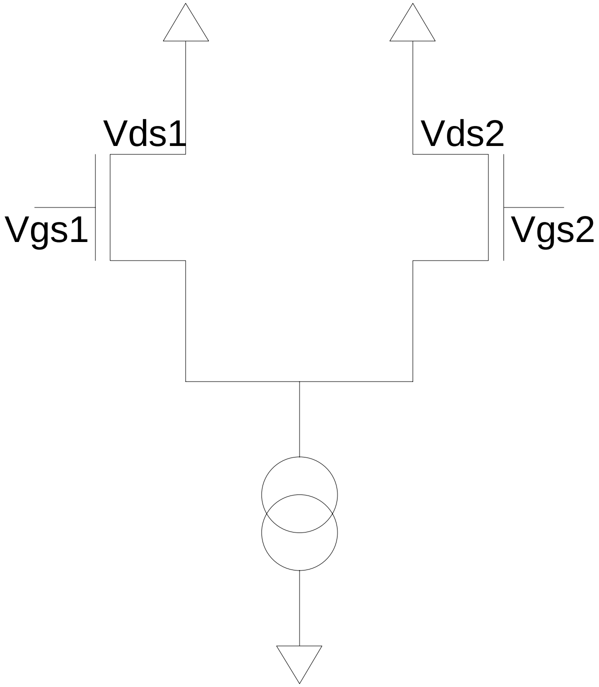
c/ <u>Stability</u>

- Example : 2 stages amplifier.
- Open loop gain : OLG = f(pole f1 and pole f2)
- Phase margin : FM = [180^o – phase(OLG = 1)]
- Stability condition : MF > 70^o
- MF ⇓ when (f2 – f1) ⇓.
- f1 depends on the parameters gds1, gm1 and C1 from 1st stage; f2 depends on the parameters gds2, gm2 and C2 from 2nd stage.
- Before irradiation, f2-f1 is large enough to assure MF > 70^o whatever may be the electrical parameters within specified limits.
- After irradiation, f1 and f2 vary differently with respect to dose
  - ⇨ (f2 – f1) is modified => MF is modified;
  - ⇨ Stability per batch can become random (loss of robustness with respect to the specified dispersion of the electrical parameters), or be totally lost.

Remedies :

- Foresee a comfortable initial phase margin (MF >80 ^{o});
- Take advantage of Miller capacity to widen f1 from f2 ;
- Make a « pole zero » compensation (addition of a zero to decrease the 180 ^{o} of the first pole and thus increase MF) ;
- Add to the OA an architecture that stabilises gm [ref. 8];
- Filters : when possible, use passive filters rather than active filters.

d/ MOS differential amplifier offset versus dose :



Dose effect :

- If the DC bias is such as Vds1 ≠ Vds2 and Vgs1 ≠ Vgs2 (example : comparator), then ΔVt1(dose) ≠ ΔVt2(dose)
  ⇨ Mismatch (Vt1-Vt2) ⇑ when dose ⇑.
- Even if the DC bias is such as Vds1 = Vds2 and Vgs1 = Vgs2 there is a local dispersion of ΔVt(dose)
  ⇨ Mismatch (Vt1-Vt2) ⇑ when dose ⇑.

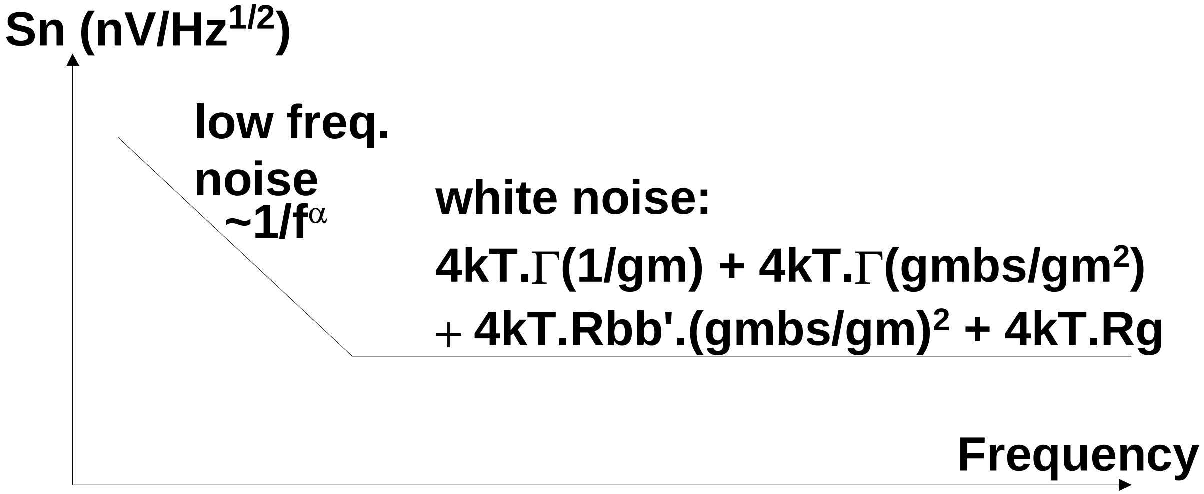
This problem concerns all the circuits that are sensitive to offsets (comparators, current mirrors, differential amplifiers, Op Amps, …)

Remedies :

- Use offset compensation schemes ;
- Replace MOS by bipolars
- If these remedies are not sufficient, use radiation-hard technologies.

Cumulated radiation effects on analogue circuits, CMOS amplifiers - continued -

e/ Noise



Sn (nV/Hz$^{1/2}$)

low freq. noise ~1/f$^{\alpha}$

white noise:

$4kT.\Gamma(1/gm) + 4kT.\Gamma(gmbs/gm^2) + 4kT.Rbb'.(gmbs/gm)^2 + 4kT.Rg$

Frequency

Input transistor spectral noise density :

Low frequency noise :

- Increases with the total dose (interface states density ⇑) ;
- Cannot be compensated by a bias adjustment ;
- Higher for NMOS then for PMOS (buried channel).

White noise :

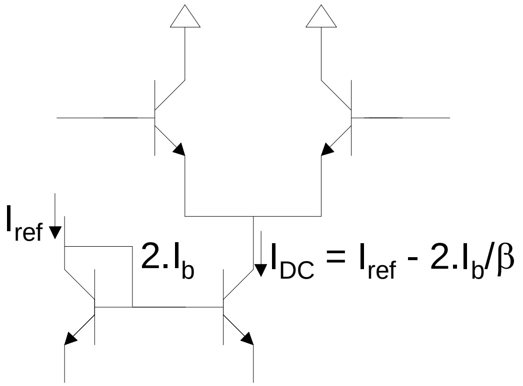
- Increases with the total dose (via gm, gmbs and Rbb')
- Can be partially compensated by a bias adjustment (gm ⇑ when I_{bias} ⇑ ; gmbs ⇓ when Vbs ⇑).

2.2. Bipolar amplifiers

Main dose effects on bipolar transistors : $\beta \Downarrow$ => Rin $\Downarrow$.

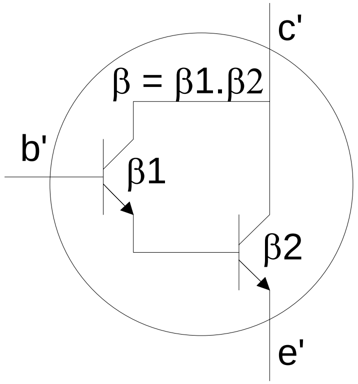
Consequences on bipolar amplifiers :

- Dose $\Uparrow$ => $\beta \Downarrow$ => Δ (DC bias) => stabilisation $\Downarrow$
  => Rin $\Downarrow$ => gain $\Downarrow$ => stabilisation $\Downarrow$
  => BW $\Downarrow$
- Dose $\Uparrow$ => $\beta \Downarrow$ => $I_{DC} \Uparrow$

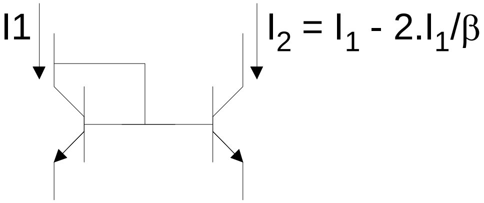


Remedies :

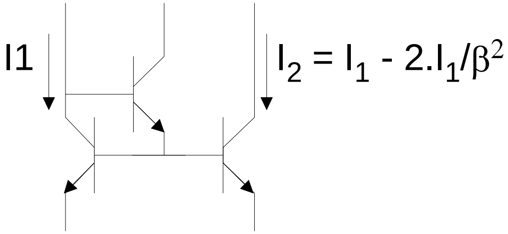
- Obtain a high gain by using a Darlington pair :
  Very high gain β => Rin remains high even after irradiation.
  Disadvantages : - Vb'e' = 2 Vbe => change in the DC bias;
  - Addition of an extra pole => stability ⇓



- Stabilise the current bias of the differential amplifier using a Wilson mirror.



Classic



Wilson

2.3. Comparators

Comparator ≡ very high gain differential amplifier.

Total dose effect :

- The stability is not a problem for the comparator, which is essentially an amplifier without feedback.
- The precision depends on the input offset, which is controlled by Vt(dose) and by gm(dose).
- The sensitivity depends on :
  - the input noise, which is controlled by gm(dose) et Rbb'(dose) ;
  - the gain gm.Rds of the amplifier, controlled by gm(dose).
- The speed depends on the gm of the transistors, controlled by dose.

Possible corrections :

- Over-size the gain in order to tolerate its reduction after irradiation without degrading the sensitivity and the speed too much;
- Raise gm by increasing I_{BIAS} (however, maintain an acceptable DC level). This is detrimental to the power consumption ;
- Offset compensation scheme ; replace MOS by bipolar ;
- Radiation hard technologies ; ...

2.4. Current mirrors

Total dose effects :

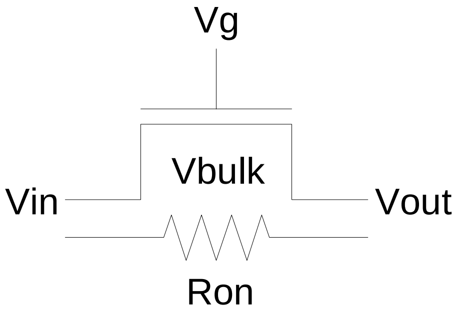
- The speed is not a problem for these circuits which are designed to provide a static current bias.
- Precision : current mirrors operate necessarily in saturated mode (Vds > Vgs-Vt). If the dose move the DC bias from the saturated mode, the current mirror loses precision.
- Precision : the mismatch of the electrical parameters (gm, Vt, β, …) induces a mismatch of the currents. It can be amplified by the dose (especially with non radiation-hard technologies).

Possible corrections :

- Raise Vdd to maintain the saturated mode ;
- Use large transistors in order to improve the matching ;
- With a bipolar technology, use Wilson mirrors ;
- If these corrections are not sufficient, use radiation-hard technologies.

2.5. Analogue switches (filters, memories, ADC, …)

- Operate in non saturated mode : Ron controlled by Vgs.
  Ron = 1/[μCox(W/L)(Vgs-Vt)] depends on Vgs(Vdd, Vin), Vt(dose), μ(dose)
- **Conditions required for normal operation :** Ron non infinite => (Vgs-Vt) ≠ 0
  ⇨ (Vdd-Vin)-Vt ≠ 0 => ***Vin < (Vdd-Vt)***
- Example : Vdd = 5V; Vto = 0.8V; Vbulk ≠ 0V => Vt ≠ Vto
  Vt = 1.8V (for ex.) => (Vdd-Vt) = 3.2V
  - Vin << 3.2V => the switch works normally ;
  - Vin ~ 3.2V => strong slowing down ;
  - Vin ≥ 3.2V => the switch stops working (Ron infini).



Total dose effects :

- ΔVt(dose) and Δμ(dose) => speed ⇓, allowed Vin ⇓, then stops working.
- I_{INTRA} can prevent NMOS from switching « OFF » completely.

Possible corrections :

- Raise Vdd ;
- NMOS with closed gate + guard ring, or PMOS (but : slow down)
- If these remedies are not sufficient, use radiation-hard technologies.

2.6. Basic rules to reduce radiation effects:

- **Current biasing** :
  Must be defined by a **reference current bias**, not by a reference *voltage* bias.

- **Voltage biasing** :
  Must be defined by a **reference voltage bias**, not by a reference *current* bias.

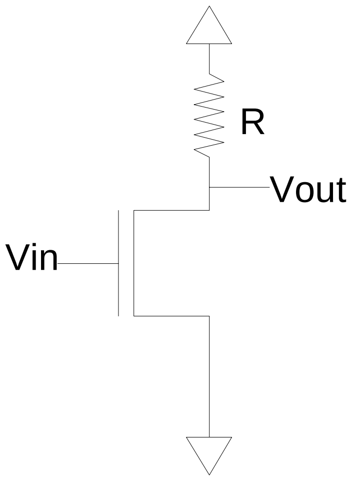
- **Differential systems :**

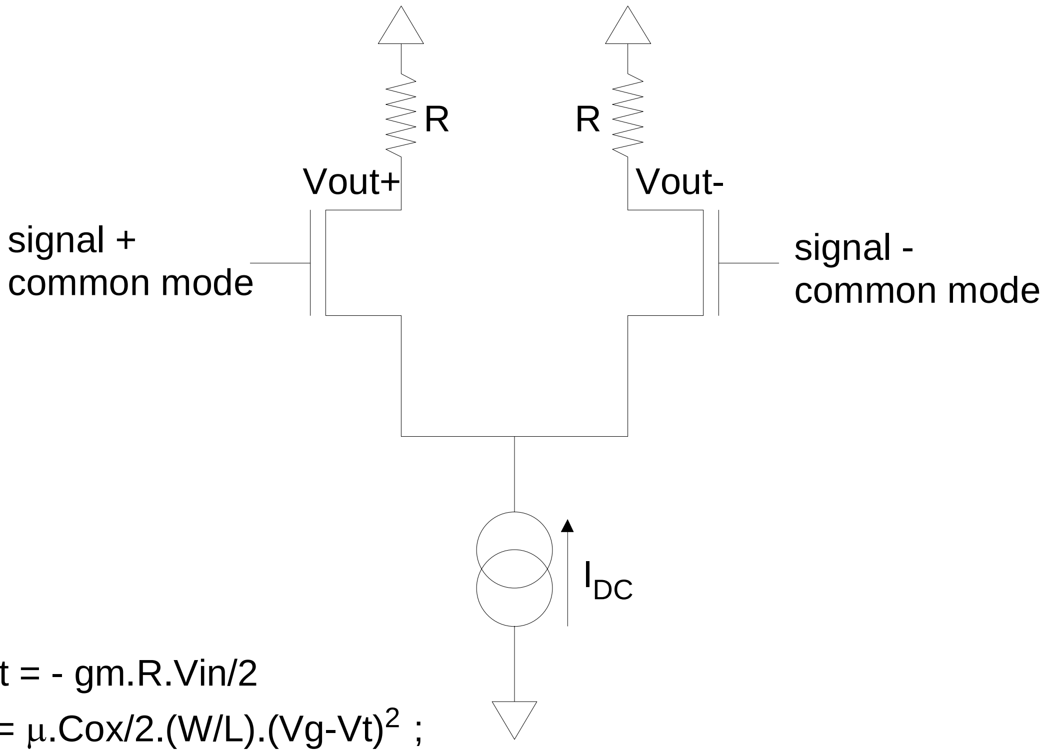
They are more robust than non differential systems because they provide a natural compensation of the voltage variations (voltage differential) or of the current variations (current differential) induced by the dose.

- **Stabilisation of the transconductance :**
  Architectures which assure the stability of $gm(I_{DC}, \mu)$ with respect to I_{DC}(dose) and to μ(dose) enable one to limit the effects of the dose dose. See for instance ref. [8] .

Cumulated radiation effects on analogue circuits, basic rules - continued -

Advantages of the differential systems:





Vout = gm.R.Vin
gm depends on Vin
=> bad

Vout = - gm.R.Vin/2

$I_{DC} = \mu.Cox/2.(W/L).(Vg-Vt)^2$;

$gm = dI_{DC}/dVg = \mu.Cox.(W/L).(Vg-Vt) = 2[\mu.Cox/2.(W/L).I_{DC}]^{1/2}$

gm determined by .I_{DC} => polarisation is not correlated with signal

If one stabilise I_{DC}(dose), gm only depends on μ(dose)

If one adjust I_{DC} to compensate $\Delta\mu$(dose), then Δgm(dose) ~ 0
The system is then reasonably hardened to the dose
However, if ΔVt is too large, compensation becomes impossible:

I_{DC} and gm shift despite the compensations ; Vgs(gm=Cte) > Vdd ; ...

Summary of the main radiation effects on analogue circuits :

Main parameters sensitive to radiation at component level :

- I_{DC} via $\Delta\mu$(dose) and ΔVt(dose) ;
- Gm via $\Delta\mu$(dose) and ΔVt(dose) or via $\Delta\mu$(dose) and Δ I_{DC}(dose) ;
- Noise
- Vt matching

Consequences at circuit level :

- Amplifiers : Δ DC bias; Δ (GBW) ; instabilities ; Δ offset ; Δ noise ;
- Comparators : Δ precision ; Δ sensitivity ; Δ speed ;
- Current mirrors : Δ precision ;
- Switches: Δ speed, Δ allowed Vin, current leakages.

Main remedies :

- Increase and stabilise Vdd and I_{DC} ;
- Comfortable phase margin ;
- Offset compensation schemes ; gm stabilisation schemes; differential structures;
- NMOS with closed gate and guard ring.

If these remedies are not sufficient, use radiation-hard technologies.

2.7. Standard methods for testing cumulated radiation effects :

Total ionising dose :

- Ionising Radiation (Total Dose) Test Procedure
  USA / DOD / MIL-STD-883E Method 1019.4 et 1019.5;
- Total Dose Steady-State Irradiation Test Method
  ESA/SCC BASIC SPECIFICATION No. 22900;
- ATLAS Policy on Radiation Hardness Assurance revision 2
  (TID test method dedicated to LHC radiation environment)

Displacement damages

- Neutron Irradiation Test Procedure
  USA / DOD / MIL-STD-883E Method 1017.2;
- ATLAS Policy on Radiation Hardness Assurance revision 2.
  (NIEL test method dedicated to LHC radiation environment)

(These test methods are suitable for both analogue and digital circuits)

3. Single Event Effects in Digital and Analogue Circuits

3.1. Definitions :

There are three families of Single Event Effects:

- **Soft SEEs:** a radiation induced transient in a linear device, or a radiation induced bit upset in a digital device. Soft SEEs are not permanent; they are cancelled by resetting the system or by rewriting data in a memory.
- **Hard SEEs:** a SEE which causes a permanent change to the operation of a device. Example: stuck bit in a memory.
- **Destructive SEEs:** a SEE which causes the destruction of a device. Example: SEL, SEB, SEGR, …

Other definitions:

- **Single Event Effect (SEE) :** Any measurable effect induced by the passage of a single highly ionising particle. This definition includes all the SEU, SHE, SEL, SEB, SEGR, … defined below.
- **Single Event Latch-up (SEL) :** Loss of functionality due to a high current state induced by a single highly ionising particle. SELs produce permanent damage unless a current limitation protects the device. In this case, the cancellation of the high current state requires a power off-on.
- **Single Event Burnout (SEB) :** Destruction of a power transistor (MOS, BJT) due to a high current state induced by a single highly ionising particle.
- **Single Event Gate rupture (SEGR) :** Destruction of a power MOS due to a conductive path and a high electrical field induced in the gate oxide by a single highly ionising particle.
- **Multi-Bit Upset (MBU) :** Multiple upset or transient induced by a single highly ionising particle.
- **Transient pulse :** transient induced by a single highly ionising particle in a linear device.

3.2. SEE types by device and by sensitive areas :

Device Type	Sensitive Area	SEU Types
Memories	Memory cells	Bit flips
	Control Logic	Bit flips if sequential, Transients if combinatorial
Combinatorial logic	Combinatorial logic	Transients
Sequential logic	Sequential logic	Bit flips
FPGAs	Combinatorial logic	Transients
	Sequential logic	Bit flips
Microprocessors	Registers, cache, sequential control logic	Bit flips
	Combinatorial control logic	Transients
ADCs, DACs	Analog portion	Transients
	Digital portion	Bit flips or transients depending on design
Linear ICs	Analog area	Transients
Photodiodes	Photodiode	Transients

(Table from reference [6])

3.3. Detection and Correction of Soft Error

EDAC = Error Detection And Correction

EDAC Method	***EDAC Capability***
Parity	*Single bit error detect*
CRC Code	*Detects if any errors occurred in a given data structure*
Hamming Code	*Single bit corrects, double bit detects*
RS Code	*Corrects consecutive and multiple bytes in error*
Convolutional encoding	*Corrects isolated burst noise in a communication stream.*
Overlying protocol	*Specific to each system implementation*

These codes can be applied for data coming from digital circuits or contained in their associated control circuits (registers, …).

They easily treat single errors, but their efficiency decreases rapidly when the error multiplicity increases.

Correction of destructive errors

- **SEGR, SEB :** Always destructive => correction by redundancy.
- **SEL :** Destruction if high current => correction by current limiter + power off-on.

Hardening by technology and by design :

- Epitaxial substrate => reduced latch-up sensitivity.
- SOI => zero latch-up
- Special layout to reduce SEU and SEL sensitivity.

3.4. Standard test methods for SEE :

- Single Event Effects Test Method and Guidelines
  ESA/SCC Basic Specification No. 25100
- ATLAS Policy on Radiation Hardness Assurance revision 2.
  (SEE test methods based on CMS and ATLAS studies [10, 11], dedicated to LHC radiation environment)

4. Summary

Total dose effect on digital circuits :

Static digital circuits :

- Switching speed ⇓;
- Static and dynamic consumption ⇑;
- No operation induced by no switching.

Dynamic digital circuits :

- Idem static digital circuits;
- No operation induced by loss of precharge.

Main remedies :

- Increase Vdd;
- Use static gates instead of dynamic gates;
- Design tricks;
- No success => use radiation-hard technologies.

Total dose effects on analogue circuits :

- Amplifiers : Δ DC bias; Δ (GBW) ; instabilities ; Δ offset ; Δ noise ;
- Comparators : Δ precision ; Δ sensitivity ; Δ speed ;
- Current mirrors : Δ precision ;
- Switches: Δ speed, Δ allowed Vin, leakage current.

Main remedies :

- Increase and stabilise Vdd and I_{DC} ;
- Comfortable phase margin ;
- Offset compensation schemes ; gm stabilisation schemes;
- Differential structures;
- NMOS with closed gate and guard ring.
- No success => use radiation-hard technologies

Single Event Effects on analogue or digital circuits:

- *Soft* : SEU, transient
- *Hard* : for example, stuck bit
- *Destructive :* SEL, SEB, SEGR, …

Main remedies :

- EDAC
- Hardening by technology (SOI, epitaxial layer)
- Hardening by design

Radiation effects on electronic circuits - continued.

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This course and other materials related to the radiation hardness assurance for LHC experiments are available on the Web site of the ATLAS Radiation Hardness Assurance Working Group:

http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm

Radiation effects on electronic circuits - continued.

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