

1 Preliminary List of Criteria for IC Design Reviews

1.1 Introduction

It is now widely accepted within ATLAS that each custom integrated circuit should undergo at least two reviews: a rather detailed Design Review and a Production Readiness Review (PRR). The primary purpose of the Design Review is to (1) flag potential deficiencies in the design at an early enough stage that improvements can be made, (2) help ensure the success of major investments such as dedicated fabrication runs, and (3) help ensure the success of the PRR. To accomplish this, the Design Review should generally be carried out at least eight months before the expected time of the PRR, which itself should occur at least several months in advance of the actual production date. The Design Review will hopefully be viewed primarily as an aid to the designers, who are the only real experts on the IC, rather than simply as a necessary bureaucratic hurdle.

Design reviews consume a significant amount of time for both the designers and the reviewers. IC's often undergo several prototyping iterations and the design may change during this process. While the optimal time to have a design review can depend on a number of circumstances, we feel that a good guideline is to have it prior to the submission of a complete IC for a dedicated fabrication run, often referred to simply as an "engineering" run. Generally the investment in an engineering run is quite large and such a run is often one of the last steps before going into production (or pre-production). Given the large amount of work involved in final chip assembly and verification, and the inevitable "schedule pressure" for submission, it may actually be useful to have the primary design review at the time that all blocks are considered finished and assembly of the chip is beginning, rather than waiting until "the chip is finished" and one is ready to submit. The advantages of this are (1) problems with individual blocks or overall design can be flagged before the entire chip is assembled and (2) plans for "top-level" verification can be reviewed in advance. It should be expected that a design review will uncover issues that need to be addressed- possibly issues that have not occurred to the designers or, more likely, issues which have occurred to the designers but have either been forgotten or left undone). In the event that the primary Design Review is held before final chip simulation and verification is complete, a "light-weight" follow-up review will be held to review final results of the top level simulation.

Design Reviews should normally be scheduled at least two months in advance as it takes considerable time to schedule a time appropriate to both reviewers and designers and documentation should be mailed at least two weeks in advance. For a complicated mixed digital/analog IC, approximately four reviewers from outside the subsystem is appropriate. For a simpler all analog or all digital chip, two outside reviewers may be adequate.

1.2 Documentation

Complete documentation for the IC should exist. It should address, at least briefly, all of the issues raised in this list of criteria for a design review. If documentation of the IC is not available, the IC is not ready for submission. We call special attention to the following items:

- Specifications of required performance and functionality
- Description of Circuit
 - Block Schematic
 - Simplified schematics of critical sub-circuits
 - Pin-out diagram and brief description of interfaces to other systems
- Summary of Overall Design Methodology
 - Identification of each major piece and its designer
 - Identification of subtle or difficult issues in each block
 - Tools used for layout and simulation of each block
 - Basic element of each block: transistor, gate, or standard cell
 - Basis of transistor models or standard cells (supplied by manufacturer, independently determined, verified by prototypes)
- Description of Procedure to Verify design is correct
 - Control of which version of each circuit block is utilized
 - Overall approach to verification of each block & top level
- Summary of tests performed if portions of the circuit have been prototyped (usually the case)
- Design techniques utilized to ensure high reliability

1.3 Specifications

A brief set of specifications for the integrated circuit should be presented. If the initial specifications for the IC were not fully met, but the performance of the circuit is considered acceptable, the specifications should be updated. Detailed specifications of the digital performance including such items as command protocols, data output format, error flagging, error recovery, power up initialization, resets, recovery from lack of synchronization, etc. should be specified.

1.4 Description of Circuit

Most integrated circuits in ATLAS are far too complicated for the detailed schematics to be useful. However a reasonably complete and accurate block diagram is very important in enabling a reviewer to understand the design methodology and verification strategy, and to spot potential problems. Simplified schematics of critical subcircuits, such as preamplifiers, receivers & drivers, delay-locked loops, DAC's, etc are likely to be useful. It may be acceptable to have these in

backup documentation as long as it is readily available. A pin-out diagram and brief description of interfaces to other systems is essential.

1.5 Description of Design Methodology

While this section can be quite brief, perhaps only a paragraph or two, it is important in guiding a reviewer to potential oversights and to the best approach to complete chip verification.

1.6 Verification of Circuit

Many of the circuits being developed for ATLAS are rather complicated and they often contain mixed analog digital circuits. Even if the function of the chip is primarily digital, low level receivers and drivers and an occasional DAC must be considered as analog objects. Often a large chip is designed by more than one designer, or blocks of circuits previously used in other IC's may be utilized. The IC's also often contain a mixture of digital sections that are the result of custom layouts together with random logic sections that may be synthesized from either standard cells or even compiled automatically at the gate level. Verification of the chip must include timing verification as well as logic verification. Simulation tools often range from (1) logic verification only using Verilog or VHDL, (2) timing verification using e.g. Verilog but with dominant capacitances "extracted" and entered into the schematic, (3) full spice simulation, including parasitic capacitances extracted from the layout. Complete verification of a chip should typically consist of the following:

- Verification of analog blocks
 - SPICE simulation
 - Protoyping (optional but recommended for high performance sections)
 - Transistor Model verification
 - Simulation with best/worst case parameters
 - Special attention to any required matching of V_{be} , β , V_t
 - Evaluation of PSRR and dependence on supply voltage
 - Have the correct I/O pads been used? Have bond wires been included in the simulation?
 - Has all functionality been simulated at the chip level rather than just at the channel level?
- Verification of digital blocks
 - Logic simulation with VHDL, Verilog or equivalent
 - Simulated at transistor level, gate level or standard cell level?
 - Timing simulation with standard cell models, gate level, or full SPICE
 - Inclusion of effects of parasitic capacitance as extracted from the layout
 - Simulation with best/worst parameters

- Logic verification of circuit at full chip level
 - Logic simulation with VHDL, Verilog, or equivalent
 - Simulation of full chip at transistor, gate, or standard cell level?
 - Behavioural models - if behavioural models are used for analog portions or memory, how is it known that behavioral model is correct?
 - Test Vector generation
 - has a rather exhaustive set of test vectors been used?
 - how was test vector "coverage" determined?
 - have test vectors corresponding to "incorrect operation" of the IC been used?
 - How is it ensured that the correct versions of each block have been used?
 - Have the correct I/O pads been used.

- Timing Verification of circuit at full chip level
 - Verilog (or equivalent) with parasitic capacitances included?
 - Verification with full spice simulation (but likely with reduced number of channels, memory locations, etc).
 - Is simulation performed from schematic or extracted netlist?
 - If from schematic, how is it known that device sizes are correct? Are parasitics included?
 - Has attention been paid to special timing, race conditions, or possible metastability (at latching of asynchronous signals for example)
 - Has simulation been performed for best/worst case models and at higher than required clock speeds?
 - Has the latest Design Kit or set of models been used?

- Layout Versus Schematic (LVS) and Electrical Rule Checking (ERC)
 - How was LVS performed?
 - How was ERC performed?
 - What discrepancies if any were ignored?

- Have all of the above been redone following the "last modification" to the circuit? If not, justify.

1.7 Prototyping and IC Characterization

- Have critical sections of the circuit been prototyped?

- Has it been shown via measurement that all performance specifications¹ are met? If not, have exceptions to the original specifications been circulated to the relevant people in the subsystem?
- Have a large enough sample of chips been tested (many tens) to verify spread in the performance?

1.8 System Tests and Testability

- If chips have been fabricated, have they been tested only on the bench or in a larger system?
- Has testability been considered in the design?
- What are the plans for production testing?

1.9 Design criteria for reliability and lifetime

Was any attention paid to minimizing impact of single point failures?

How is it ensured that the all parameters in the design are adequately far from the "maximum allowed values" In particular has one verified that adequate metal is used for power distribution?

Has ESD protection been included? If not, what handling procedures have been developed to prevent damage.

Were any techniques used to enhance reliability (multiple vias, wider than nominal widths, clearances, etc.)

Is there data on chip lifetime from the manufacturer?

Has the process been used in a similar way for other circuits?

How has a package or other sealant been selected? Is it known what impact this may have on chip lifetime? Is an adequate number of power supply and ground pins utilized?

1.10 Effect of Radiation environment

- Has the process been verified as sufficiently radiation hard?
- Have any prototype chips been tested beyond full expected dose?
- Have low dose rate effects been evaluated for both transistors and resistors?
- Has simulation been performed for worst case process parameters plus the effects of radiation?

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