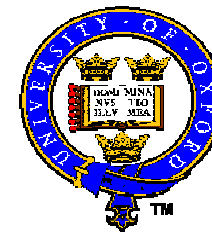


# *Atlas SCT Barrel Harness Production Testing*

**Jan Troska – [j.k.troska@rl.ac.uk](mailto:j.k.troska@rl.ac.uk)**

*Rutherford Appleton Laboratory*

*Senerath Galagedera, Martin Morrissey, Dave White, Robert Millea, Tim Hayler, Tony Weidberg*





# Overview

- ① **Project description**
  - ✦ *Component descriptions*
  - ✦ *Harness description*
- ② **Testing overview**
  - ☆ *Individual components*
  - ☆ *Component tests*
  - ☆ *Harness tests*
- ③ **Testing schedule**
- ④ **Conclusions**





# Project Description

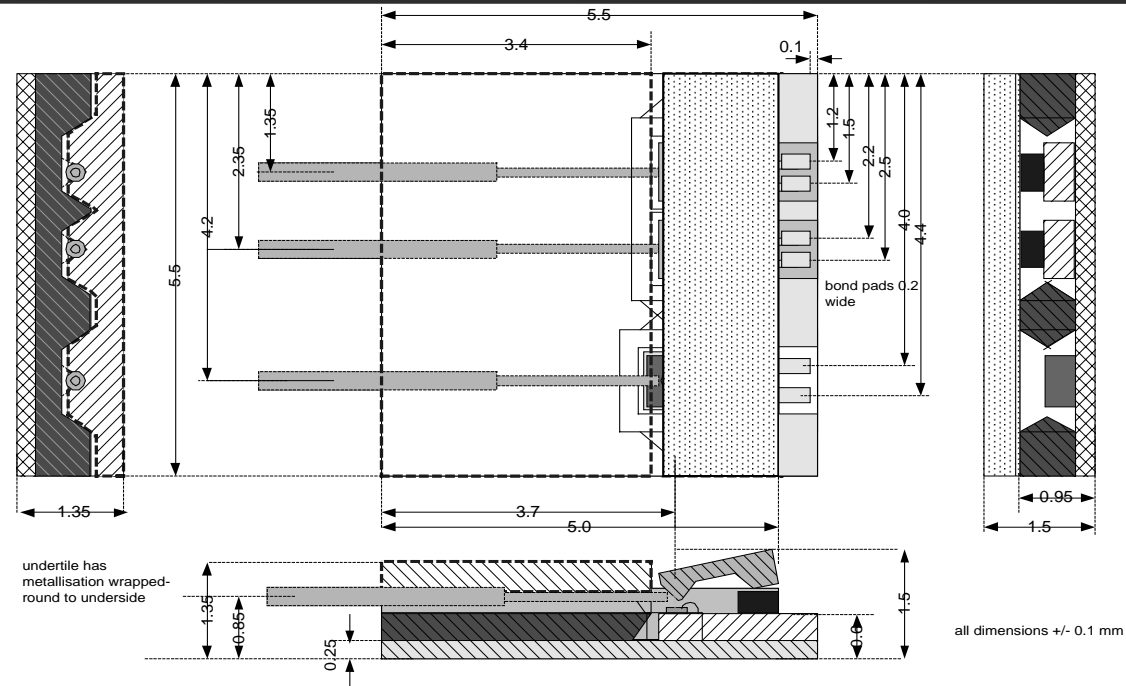
## ❖ What is a Barrel Harness?

- ✓ *Provides power, clock and command to silicon modules and allows readout*
- ✓ *Consists of several components*
  - ⇒ *Opto-package (GEC-Marconi development as baseline)*
  - ⇒ *Driver ASIC: VDC*
  - ⇒ *Receiver ASIC: DORIC*
  - ⇒ *Flex-rigid interconnection piece: Dog-leg*
  - ⇒ *Al-Kapton Power Tape*

## ❖ Why test them?

- ✓ *Need to populate barrels with working units*
- ✓ *Need to assure assemblies function within specifications over operational temperature range*





Silicon packaged VCSEL-PIN unit - schematic showing proposed key dimensions - prepared by J. Hall 25.3.99 - Marconi Materials Technology, Caswell

**N.b.**  
Not pigtailed  
by GMMT  
(lids separate)

## ❖ Custom development by GEC-Marconi (GMMT)

## ❖ Silicon undertile carries:

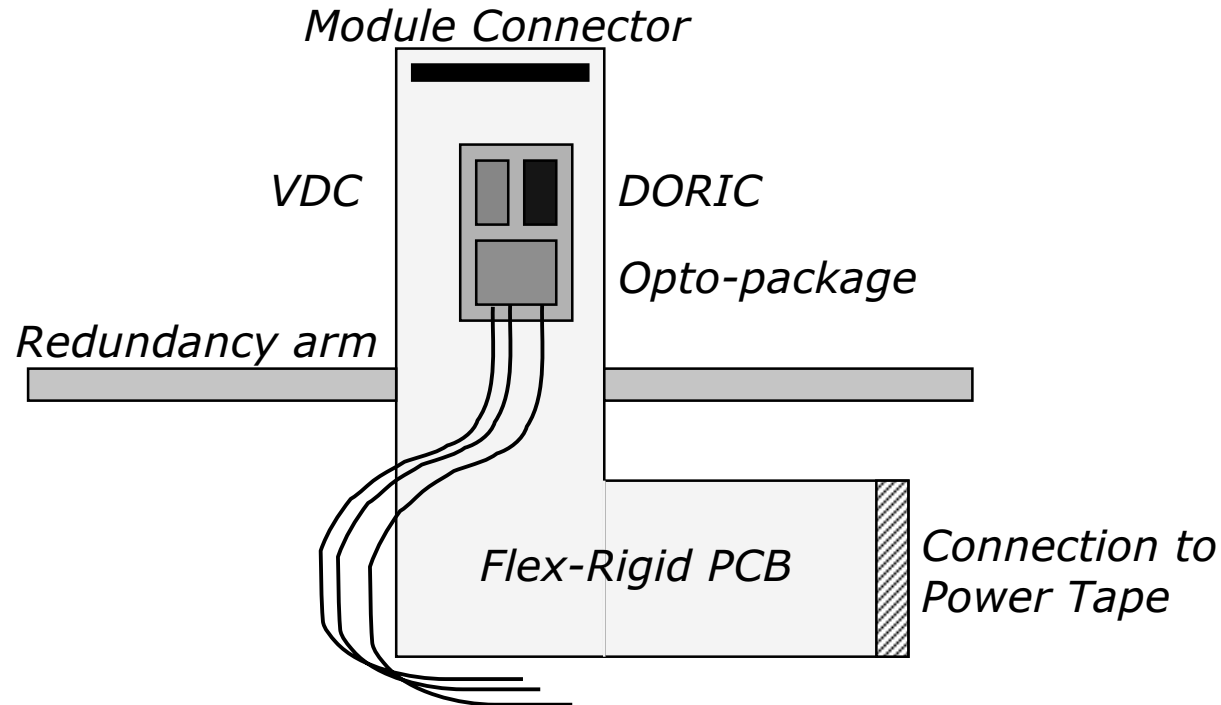
- 2 VCSELs (Mitel as baseline)
- 1 Epitaxial Silicon p-i-n photodiode (Centronics as baseline)

## ❖ VCSEL Driver Chip (VDC)

- ⇒ *Provides a constant bleed current to pre-bias the VCSEL*
- ⇒ *Takes LVDS input from the module and converts it into a current pulse to drive the VCSEL*
- ⇒ *Allows adjustment of output signal height*

## ❖ Digital Optical Receiver Integrated Circuit (DORIC)

- ⇒ *Amplifies clock and command signals received by p-i-n photodiode*
- ⇒ *Decodes the bi-phase mark encoded signals into separate clock and command data-streams*
- ⇒ *Outputs clock and command data-streams as LVDS signals to the module (and its nearest neighbour)*



**N.b.**  
Design still  
under evaluation

- ❖ Makes 90° turn of power tape to allow connection to module
- ❖ Carries Opto-package, VDC and DORIC
- ❖ Solder connection to Al/Kapton power tape
- ❖ Solder connection to nearest neighbours for redundancy



# *Barrel Harness*

- ❖ **Covers one half of a barrel and provides control, readout and power to six modules**
- ❖ **Two types of connection**
  - ① *Electrical (Power Tapes)*
  - ② *Optical (Optical Fibre Ribbon)*
- ❖ **Per harness**
  - ⇒ *6x Power Tapes*
  - ⇒ *1x 12-way fibre ribbon (Readout Data)*
  - ⇒ *1x 6-way fibre ribbon (Clock and Command signals)*





# Testing Overview

- ❖ **Assure testing occurs to verify in-spec operation of all components over the range of operating conditions (V,L,T)**
- ❖ **Electrical tests**
  - ⇒ *Continuity*
  - ⇒ *Voltage drop & Breakdown*
  - ⇒ *Power Cycling*
- ❖ **Opto-electronic tests**
  - ⇒ *Bit Error Rate (BER)*
  - ⇒ *Minimum received optical power to ensure operation (S-curve)*
- ❖ **Temperature tests**
  - ⇒ *Soak test at realistic operating temperatures*
  - ⇒ *Temperature cycle between room temperature and low temperature*  
*Number of times foreseen during Atlas lifetime*





# Testing Opto-packages

- ❖ **Component Test and Burn-in**
  - ✓ *Carried out by manufacturer (Mitel & Centronics)*
- ❖ **Whole package will undergo DC test at GMMT before delivery**
- ❖ **In-house testing required?**
  - ✓ *Wait until lids mounted*





# Testing Dog-legs

## ❖ Individual Dog-legs tested by manufacturer

- ✓ *Visual inspection*
- ✓ *Continuity*
- ✓ *Resistivity & Voltage drop*

## ❖ Solder to Al/Kapton power tape

- ⇒ *Re-measure*
  - ✓ *Continuity*
  - ✓ *Voltage Drop*

## ❖ Mount Opto-package, VDC and DORIC





# Testing Harnesses

- ❖ **More comprehensive acceptance test required**
- ❖ **Detailed test of functionality in both data channels and clock & command channel**
  - ⇒ *Minimum optical power required for operation (S-curve)*
  - ⇒ *BER test at nominal power*
- ❖ **Soak test at room- and low-temperature**
  - ⇒ *Constant (nominal) PSU output*
  - ⇒ *Vary PSU output within specifications*
- ❖ **Cycle temperatures and repeat test**
  - ⇒ *Power off during cycling*





# *Preliminary Schedule*

- ❖ **Preliminary design review (testing schedules defined)**
  - ⇒ *Late July 1999*
- ❖ **Installation of test system**
  - ⇒ *November 1999*
- ❖ **Test system with small number of channels (enough for one harness)**
  - ⇒ *Start 2000*
- ❖ **Full system available for production testing**
  - ⇒ *April 2000*





# Conclusions

- ✓ **SCT Barrel harness testing is becoming better defined**
- ✓ **Design of test system (and components) is being started**
- ❖ **Testing is closely linked to final designs of components being established**
  - ⇒ *Ideas are converging*
- ✓ **Testing scenarios are sufficiently flexible to allow re-definition should it become necessary**

