1 SPI serial bus master channel with 8 individual slave select lines. The Serial Peripheral Interface (SPI) channel implements a full duplex synchronous serial bus master with a single transaction length of up to 128 bits and a programmable transfer rate up to 20 MHz. It supports all the standard SPI bus operating modes: 00, 01, 10 and 11. It also integrates 8 independent slave-select lines. The bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps. The SPI channel is implemented around a 128-bit shift register that serializes and de-serializes the bit-streams between the MISO and MOSI SPI lines and the internal parallel bus. The SPI channel is protocol agnostic. The user specific protocol is implemented in FPGA circuitry residing at the control room electronics. The SPI channel can be powered down to conserve power.

1 JTAG serial bus master channel. The JTAG channel can perform bus transactions of up to 128-bit length. Longer transactions are also possible by segmenting them and having them executed on consecutive channel commands. The interface implements an asynchronous reset line of configurable pulse width. The bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps. The JTAG channel is implemented around two 128-bit shift register that serializes and deserializes the bit-streams between the TMS, TDO and TDI lines and the internal parallel bus. The JTAG channel in the SCA does not implement a JTAG – 4 –